

Design of ultra low noise amplifiers

Vojtěch Janásek, www.janascard.cz

(update 1/2012, 10/2013, 5/2015)

Various types of ultra-low noise amplifiers both for DC and AC signals are described. “Ultra-low noise” here means that voltage noise density is below 1 nV/sqrtHz for AC amplifiers or noise less than 100 nVpp for DC amplifiers.

1. Ultra-low noise AC amplifiers

Op amplifiers (OA) are widely used as AC amplifiers. For ultra-low noise amplifiers are suitable especially LT1028 or LT1128 (old but the lowest noise available OA as far as I know) from Linear Technology (www.linear.com) or ADA4898 or AD8597 from Analog Devices (www.analog.com). Both amplifiers have voltage noise density at 1 kHz around 1 nV/sqrtHz and also offers excellent DC precision. TI (www.ti.com) offers some very low noise amplifiers like OPA211 with noise 1.1 nV/sqrt at supply current 3.6 mA from 5 V and LME49990 with very low distortion. Maxim (www.maxim-ic.com) offers MAX9632 with noise below 1nV/sqrt Hz.

OA have also some drawbacks: 1. input differential stage has voltage noise density $\sqrt{2}$ times increased against simple input transistor.

2. Ultra low noise OA usually require at least 10 V (+-5V) supply voltage and supply current is often more than 5 mA. If only AC amplification is necessary, it is possible to design a lower noise discrete amplifier with lower power consumption and lower cost.

1.1 Ultra-low noise AC amplifiers with bipolar transistors

With bipolar transistors, the value for emitter-base voltage noise and base current noise of an ideal transistor can be expressed as follows [1],[2]:

$$e_n = kT \sqrt{\frac{2}{qI_c}}, i_n = \sqrt{2qI_b} = \sqrt{\frac{2qI_c}{h_{FE}}} \quad (1)$$

With real transistor, additional noise source which can be modeled as additional resistor r_{bb} must be added. The third noise source is base current noise which flows through source resistance r_s . So total noise of a transistor connected to voltage source with resistance r_s can be expressed as:

$$e_N = \sqrt{e_n^2 + 4kTr_s + i_n^2 r_s^2} = \sqrt{\frac{2k^2 T^2}{qI_c} + 4kTr_s + \frac{2qI_c}{h_{FE}} r_s^2} \quad (2)$$

For low source impedance, the r_{bb} of transistor should be added to source impedance r_s .

To find the collector current which yield the minimum overall equivalent input noise with a given source impedance, the last formula can be differentiated with respect to I_c and set equal to zero [2] and gives:

$$I_c(opt) = \frac{kT}{q} \frac{\sqrt{h_{FE}}}{r_s} \quad (3)$$

For accurate calculation keep in mind that h_{FE} isn't constant and also depends on I_c .

Formulas (2),(3) are clear but in practice the main problem is that value of r_{bb} isn't specified in nearly any transistor data sheet. The noise of transistor is usually described as noise figure measured at low current (usually about 100 uA or less) with relatively high source resistance and doesn't help here very much. SPICE simulation must be also used very carefully because available models don't reflect noise performance correctly. Voltage noise density of a low noise BC549 at collector current 10 mA was simulated with 3 different models – ORCAD's

built in model, model from Philips and model from Fairchild. Three totally different results were obtained: 0.12 nV/sqrtHz, 0.19 nV/sqrtHz and 1.3 nV/sqrtHz and corresponding r_{bb} is 0 Ohm, 1 Ohm and 100 Ohm. The last value is the closest to reality. That measurement also shows that so called “low noise” transistors are not suitable for really low noise applications at higher collector current due their high r_{bb} value. It can be expected that transistors with higher I_{cmax} have also lower r_{bb} , so several transistors with higher I_{cmax} were measured. Commonly available transistors like 2N3904, 2N2222, BC337, BC817,BCP68 were tested. All that transistors had lower noise at $I_c=1.3$ mA than BC549. The lowest noise was obtained with the BC337 ($r_{bb}=30$ Ohms). Update 5/2015 – nearly perfect low noise transistor is 2SC3324 (PNP version is 2SA1312) with specified noise at higher I_c . R_{bb} is only 20 Ohms and h_{fe} up 700 so input noise current is also very low.

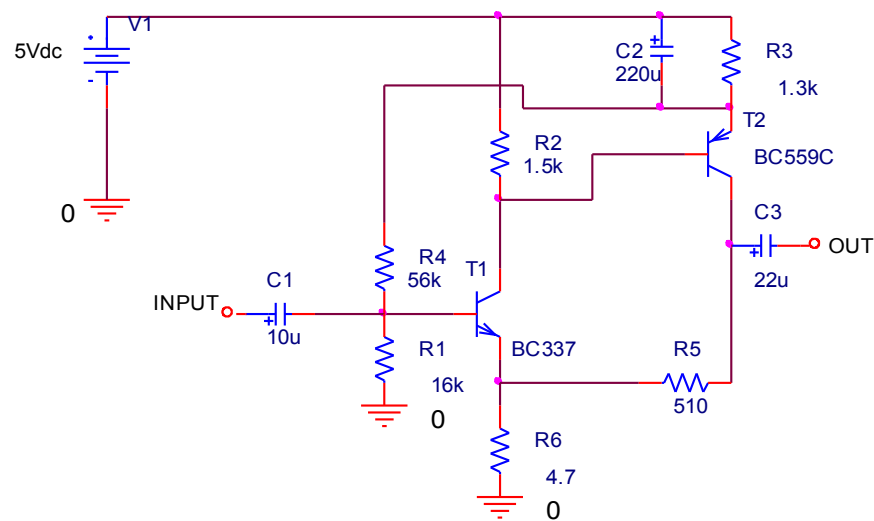


Fig.1. An ultra-low noise AC amplifier

The Fig. 1. shows a practical example - an ultra low noise amplifier with gain 100 based on BC337 derived from [2]. Although very simple, the amplifier has input noise below 0.7 nV/sqrtHz – lower than any monolithic OA and requires only 3 mA from 5 V supply. Gain is set by the ratio of R_5/R_6 , noise of R_6 is added to input noise so low value 4.7k is used. Small signal bandwidth exceeds 1 MHz. This simple approach has also some drawbacks, the main is that output voltage swing is limited to only several hundred mV. Open loop gain of the amplifier is only 60 dB, so gain accuracy, distortion performance and output impedance is worse compared to OA. Flexibility is a big advantage of the circuit – increasing resistors $R_1=160k$, $R_2=27k$, $R_3=22k$, $R_4=560k$, $R_5=2.4k$, $R_6=22$ reduces supply current to 200 uA and voltage noise density is still only 1.7 nV/sqrtHz, it is about 10 times lower than a OA with the same current consumption. Small signal bandwidth exceeds 100 kHz, it is also very good value for a such low power circuit.

An improved version of the ultra low noise amplifier is shown in Fig.2. PNP transistor was replaced with OA. Q_1 's collector voltage is set by resistor divider R_7/R_6 , bias point is controlled via DC feedback path R_2 . The noise contribution of the U1 can be neglected if its noise density is lower than $e_n \cdot A_u / 3$ where e_n is voltage noise density of input transistor, A_u is gain of the input stage, $A_u = 40 \cdot I_c \cdot R_3$. With values shown in Fig.2, amplifier with noise density below 20 nV/sqrtHz should be used. Gain is precisely set by divider $R_2 / (R_1 \parallel R_9)$, gain up 10000 is possible due high open loop gain of the U1. Distortion and output

impedance is also greatly reduced over previous circuit. Low frequency corner is given by $R1C4$. DC bias of $C4$ is below 100 mV so low voltage low ESR type can be used.

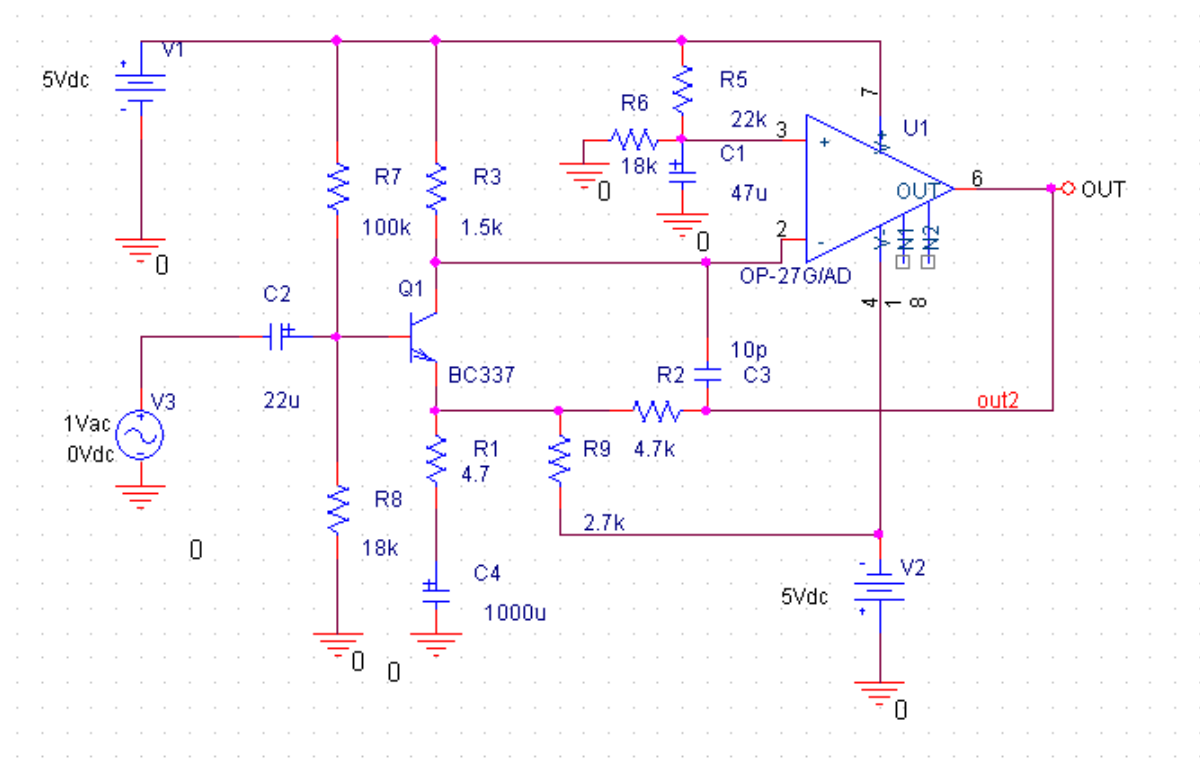


Fig.2. An improved version of ultra-low noise amplifier

Both circuits have voltage noise density around $0.7 \text{ nV}/\sqrt{\text{Hz}}$, if lower noise density is required, input transistors can be simply paralleled. If N transistors are used, noise is \sqrt{N} reduced and result can be modeled as one transistor with $r_{bb}' = r_{bb}/N$ and $I_{c}' = N * I_{c}$. This approach has also some drawbacks - base current noise is \sqrt{N} times increased and transistors must be matched. Matched monolithic pairs are available from several vendors, for instance LM394 from National Semiconductors (www.national.com) or MAT-01, MAT-02, MAT-03 from Analog Devices. The matched pairs have also very low and fully specified noise at higher collector current. If more transistors are necessary, matched quad THAT300 from THAT corporation (www.thatcorp.com) is available. The main disadvantage of the matched transistors is high price. Transistors needn't be matched with high accuracy, 20% difference in collector current is acceptable, so raw selection (or no selection) of BC337(2SC3324) can be done. If no selection is used, equalization emitter resistors 100 Ohm with blocking capacitor 470 uF in every emitter reduce differences between transistors – Fig . 3.

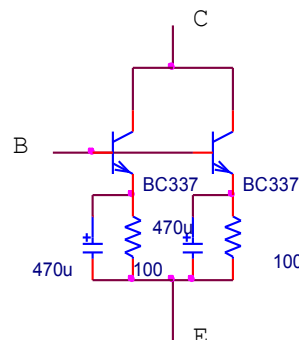


Fig. 3. Paralleling with balancing emitter resistors

1.2 Ultra-low noise AC amplifiers with unipolar transistors

Amplifiers with bipolar transistor offer very low noise but have also some drawbacks – low input impedance and high input current noise, so they are suitable especially for signal sources with low output impedance, typically below 1 k Ω .

If high input impedance or very low input noise current is necessary, an input stage with unipolar transistors is a better choice. OAs with FET inputs exist, but their noise is significantly worse than with bipolar ones – e_n is usually higher than 4 nV/ $\sqrt{\text{Hz}}$. Examples are JFET OPA827 from TI or CMOS AD8655, AD8656 from Analog Dev, MAX4475 from Maxim or JFET LT1792 from Linear Technology.

Unipolar transistors in ultra low noise applications have two disadvantages: 1/f noise corner is relatively high – usually more than 1 kHz (bipolar transistors have 1/f noise corner some Hz or tens Hz) and voltage noise density is relatively high – usually some nV/ $\sqrt{\text{Hz}}$ or more.

Noise of the unipolar transistor can be modeled as a noise of the resistor with value $1/Y_{fs}$, so transistors with high transfer admittance and usually high I_{dss} are good candidates for low noise applications.

Fortunately there are a few types with very low noise. That is an ultra low noise JFET 2SK170 and 2SK369 from Toshiba (now obsolete) or equivalent LSK170 from Linear Systems (www.linearsystems.com) [5] with voltage noise density below 1 nV/ $\sqrt{\text{Hz}}$. BF862 from Philips is another excellent choice but its noise is specified at 100 kHz. InterFET introduces very low noise IF9030 and IF3601 with noise density 0.5 and 0.3 nV/ $\sqrt{\text{Hz}}$ respectively but they have large capacitances and they are quite expensive so using more BF862 in parallel may be a better option. Fig. 4. shows an ultra-low noise amplifier with two JFETs 2SK170 with gain 100 and voltage noise density below 0.7 nV/ $\sqrt{\text{Hz}}$.

As with bipolar transistor, T3 can be replaced with OA, but care must be taken because voltage gain of the input stage $A_u = Y_{fs} * R_2$ is usually lower than with bipolar transistor at the same I_c , so a low noise OA must be used. If lower noise than 1 nV/ $\sqrt{\text{Hz}}$ is necessary, JFETs can be paralleled as shown on Fig.4. If only two transistors are necessary, matched pair LSK289 from Linear Systems is a good choice.

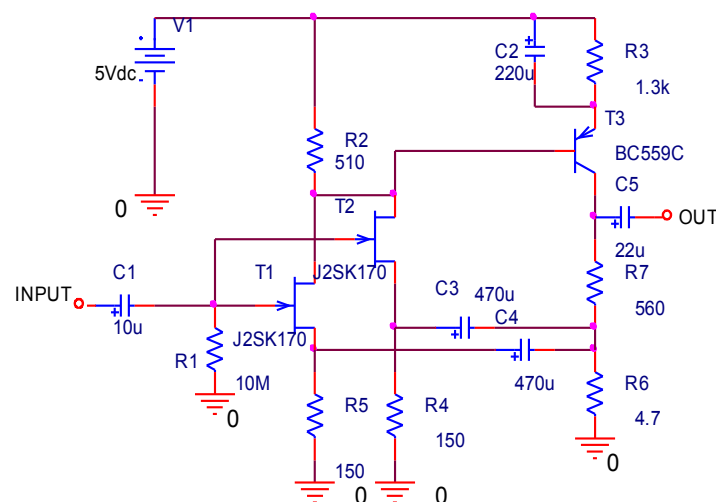


Fig. 4. An ultra low noise amplifier with FET

Matching of single transistors is more difficult than with bipolars due to wider spread of I_{dss} between JFETs, so it is usually simpler to set DC bias point for every transistor separately and use AC feedback only as shown on Fig 4. Drawback of no DC feedback is worse bias point stability and accuracy, so it can be necessary to replace R2 with trimmer 1k and set T3 U_{ce} to 2.5V-3.0 V.

The big advantage against bipolar transistors is that there is nearly no input current noise so it is simple to connect in parallel as many transistors as necessary. The limit is only power

consumption and increased input and feedback capacitance. If low input capacitance and high bandwidth is important, BF862 is the best choice.

2. Ultra-low noise DC amplifiers

For accurate amplification of small DC signals, amplifiers with low offset, low offset drift and low noise are necessary. The best choice between bipolar OA are the same OAs as for AC amplifiers. If even better parameters are necessary, chopper or autozero amplifiers must be used. There is a lot of monolithic chopper or autozero amplifiers with excellent offset and offset drift performance but noise performance is much worse than with mentioned bipolar OA although the main noise source – $1/f$ noise is removed. Typical values are more than 20 nV/sqrtHz. Fortunately some new amplifiers with improved performance appear, actually it is ADA4528 with en 5.6 nV/sqrtHz

Better results can be obtained with discrete chopper amplifier described above.

This chopper amplifier is based on a 40 nVpp Chopped FET Amplifier [3],[4] but it is significantly improved. It has lower noise, power consumption and component count. The main difference is a very low noise AC amplifier composed by T1 and T2, see Fig.5. The excellent noise performance is given by T1 – 2SK170 operating with I_d current about 2 mA and with noise density below 1nV/sqrtHz. Total gain of the AC amplifier is given by resistors R2 and R5 and is approximately 1000 for $R5 = 1$ kOhm, aprox. 3000 for $R5=4k7$.

The noise and offset performance of the chopped amplifier is also affected by the input modulator. MAX4693 (U1A) is used here because it has very low R_{on} 20 Ohm and very low charge injection 2 pC. U1B acts as an output demodulator and demodulated signal is then integrated by U2. Total DC gain (1000) is set by R8,R9 ratio. Noise of the R9 directly affect total noise so very low value 1 Ohm is used here.

As a clock source CD4060 is used with a quartz 32.768 kHz which produces accurate and stable frequency 1024 Hz. This frequency is harmonically unrelated to 50 Hz. It will be better

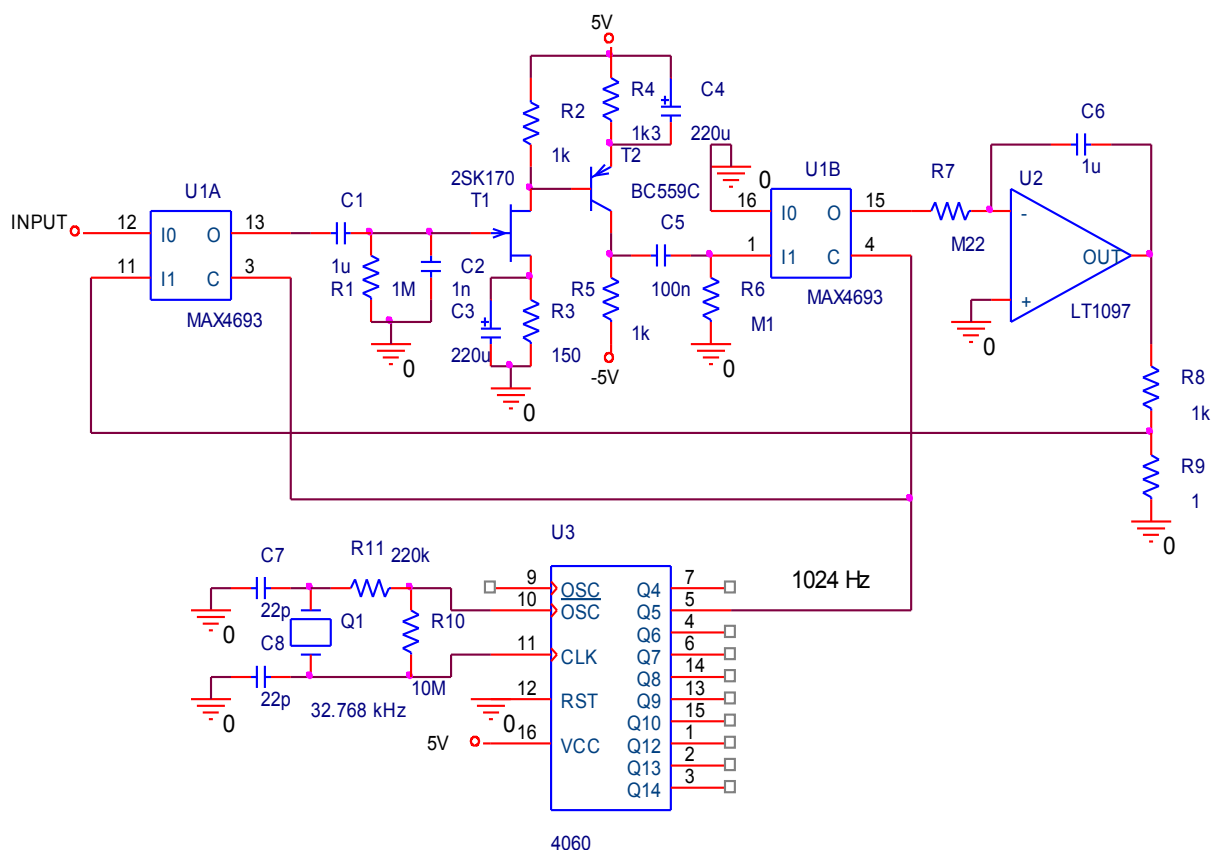


Figure 5. A chopper amplifier with noise 8 nVpp

to use different frequency for 60 Hz suppression.

Total bandwidth is given by the gain of the AC amplifier and time constant of the integrator (R7,C6). With values in Fig.1 and AC gain 1000 (R5=1k) the bandwidth is aprox. 0.2 Hz and is the same as original [3],[4]. Increasing value of R5 to 4k7 gives wider bandwidth 0.6 Hz and also lower offset voltage. If wider or narrowed bandwidth is required, C6 can be changed accordingly. Fig. 6 shows measured noise on the output of the amplifier with AC gain 1000 (R5=1k) during 60 s time window. A DAQ card AD14PCI with additional amplifier and software Adcontrol was used. Total noise referred to input is 8 nVpp or 1.4 nVef, it is aprox. 5 times improvement against original [3],[4]. Sampling period of the DSP integrating AD converter is 40 ms, so measured bandwidth is about 10 Hz, but noise bandwidth is limited by the chopper amplifier to $1.57 \times 0.2 \text{ Hz} = 0.3 \text{ Hz}$ and voltage noise density e_n is 2.6 nV/sqrt Hz. As with every chopped amplifier there is no 1/f noise component so total noise for different bandwidth can be simply expressed as

$$U_n = e_n \sqrt{f_s} \quad (4)$$

where f_s is noise bandwidth – for 1. order low pass $f_s = 1.57 \times f_{-3dB}$

e_n - voltage noise density - 2.6 nV/sqrtHz

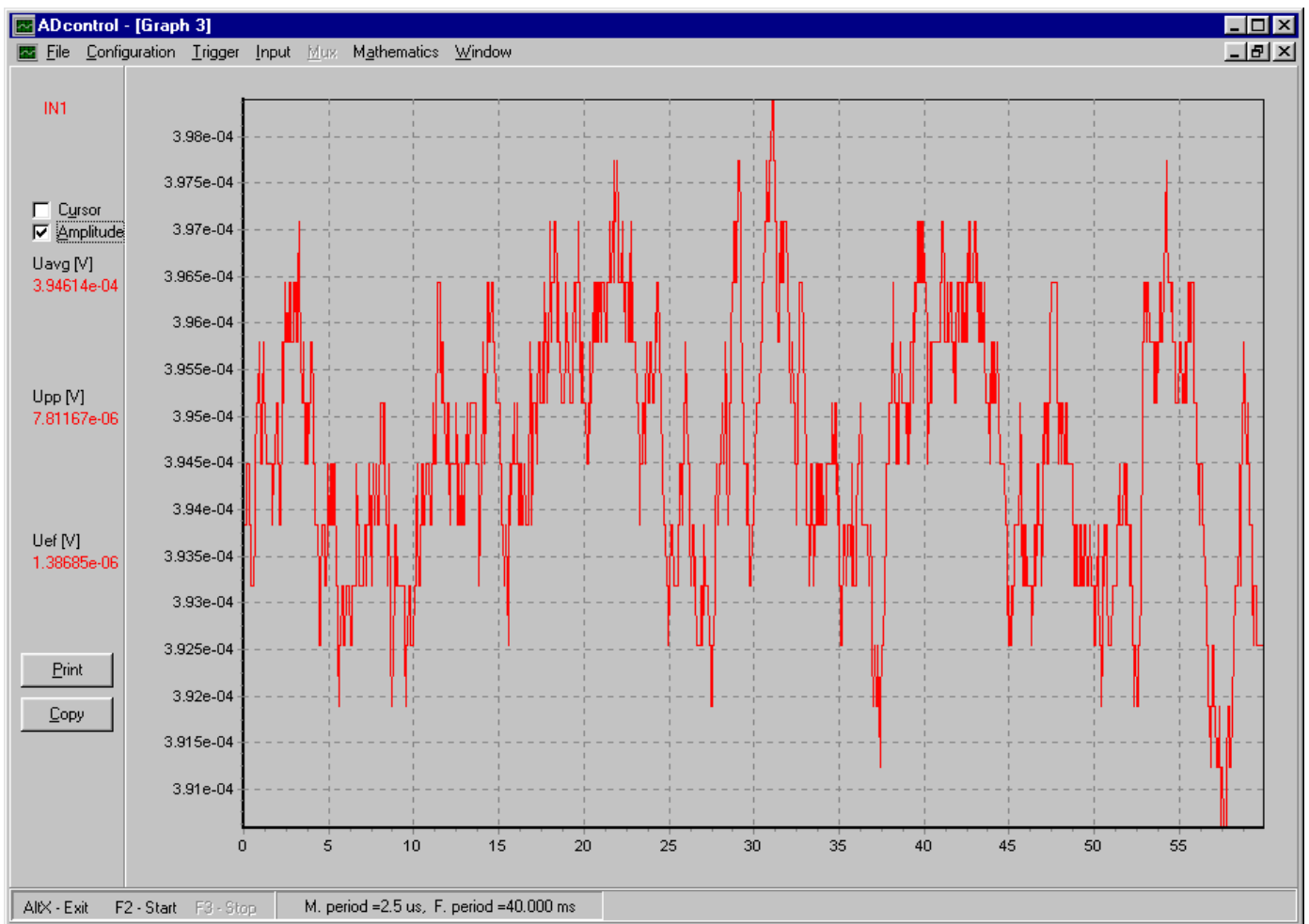


Figure 6. Output noise in 60 s sample period

3. Instrumentation amplifiers

Instrumentation amplifiers are used for amplification of differential signals typically from bridge sensors like strain gauges. Offer of ultra low noise monolithic instrumentation amplifiers isn't wide, it is only INA103 and less expensive INA163 from TI, both have en 1 nV/sqrtHz. THAT offers similar THAT1510 with wider bandwidth. AD8429 from AD offers full DC specification and lower input currents at expense of higher input current noise.

4. Practical recommendations for design of low noise amplifiers

Every resistor is a noise source so it is necessary to keep all resistors in a signal path (and also signal source resistance) on very low level otherwise low noise performance of any amplifier will be wasted. Proper supply decoupling (omitted for clarity) is necessary. Parallel combination of large electrolytic cap 470uF with 22uF tantalum and several 100nF ceramic in every supply with serial resistor 47-100 Ohm is recommended. If switching regulators are used, additional RC/LC filter is essential. A PCB with at least 2 layers and solid ground plane is strongly advised. Electrostatic and magnetic shielding is also useful especially in noisy environment. For DC amplifiers, a circuit must be also well shielded from air currents to eliminate the possibility of thermoelectric effects. Every connection of two different metals creates thermocouple with sensitivity 1-10 uV/K, so temperature change only 0.01 deg.C gives 10-100 nV, up to 10 times more then the noise of the described chopper amplifier!

5. References

- [1] Dostál Jiří, Operační zesilovače, SNTL Praha 1981
- [2] National Semiconductors, AN-222 - Super Matched Bipolar Transistor Pair Sets New Standards for Drift and noise, <http://www.national.com/an/AN/AN-222.pdf#page=10>
- [3] Williams Jim, Linear Technology Application Note 93
<http://www.linear.com/pc/downloadDocument.do?navId=H0,C1,C1010,D4182>
- [4] Williams Jim, Linear Technology Magazine March 2006 p.39,
http://www.linear.com/lmagazine/LTMag_V16N1_Mar06.pdf
- [5] <http://www.linearsystems.com/datasheets/LSK170.pdf>