

775 Nanovolt Noise Measurement for A Low Noise Voltage Reference

Quantifying Silence

Jim Williams

Introduction

Frequently, voltage reference stability and noise define measurement limits in instrumentation systems. In particular, reference noise often sets stable resolution limits. Reference voltages have decreased with the continuing drop in system power supply voltages, making reference noise increasingly important. The compressed signal processing range mandates a commensurate reduction in reference noise to maintain resolution. Noise ultimately translates into quantization uncertainty in A to D converters, introducing jitter in applications such as scales, inertial navigation systems, infrared thermography, DVMs and medical imaging apparatus. A new low voltage reference, the LTC6655, has only 0.3ppm (775nV) noise at 2.5V_{OUT}. Figure 1 lists salient specifications in tabular form. Accuracy and temperature coefficient are characteristic of high grade, low voltage references. 0.1Hz to 10Hz noise, particularly noteworthy, is unequalled by any low voltage electronic reference.

Noise Measurement

Special techniques are required to verify the LTC6655's extremely low noise. Figure 2's approach appears innocently straightforward but practical implementation represents a high order difficulty measurement. This 0.1Hz to 10Hz noise

testing scheme includes a low noise pre-amplifier, filters and a peak-to-peak noise detector. The pre-amplifier's 160nV noise floor, enabling accurate measurement, requires special design and layout techniques. A forward gain of 10⁶ permits readout by conventional instruments.

Figure 3's detailed schematic reveals some considerations required to achieve the 160nV noise floor. The reference's DC potential is stripped by the 1300μF, 1.2k resistor combination; AC content is fed to Q1. Q1-Q2, extraordinarily low noise J-FET's, are DC stabilized by A1, with A2 providing a single-ended output. Resistive feedback from A2 stabilizes the configuration at a gain of 10,000. A2's output is routed to amplifier-filter A3-A4 which provides 0.1Hz to 10Hz response at a gain of 100. A5-A8 comprise a peak-to-peak noise detector read out by a DVM at a scale factor of 1 volt/microvolt. The peak-to-peak noise detector provides high accuracy measurement, eliminating tedious interpretation of an oscilloscope display. Instantaneous noise value is supplied by the indicated output to a monitoring oscilloscope. The 74C221 one-shot, triggered by the oscilloscope sweep gate, resets the peak-to-peak noise detector at the end of each oscilloscope 10-second sweep.

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LTC6655 Reference Tabular Specifications

SPECIFICATION	LIMITS
Output Voltages	1.250, 2.048, 2.500, 3.000, 3.300, 4.096, 5.000
Initial Accuracy	0.025%, 0.05%
Temperature Coefficient	2ppm/°C, 5ppm/°C
0.1Hz to 10Hz Noise	0.775μV at V _{OUT} = 2.500V, Peak-to-Peak Noise is within this Figure in 90% of 1000 Ten Second Measurement Intervals
Additional Characteristics	5ppm/Volt Line Regulation, 500mV Dropout, Shutdown Pin, I _{SUPPLY} = 5mA, V _{IN} = V _O + 0.5V to 13.2V _{MAX} , I _{OUT(SINK/SOURCE)} = ±5mA, I _{SHORT Circuit} = 15mA.

Figure 1. LTC6655 Accuracy and Temperature Coefficient Are Characteristic of High Grade, Low Voltage References. 0.1Hz to 10Hz Noise, Particularly Noteworthy, Is Unequalled by Any Low Voltage Electronic Reference

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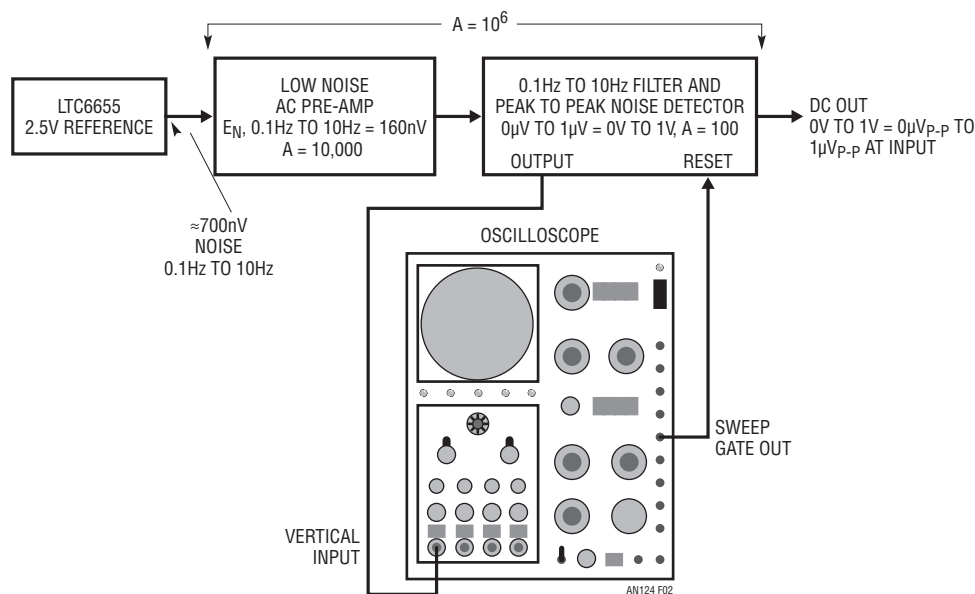


Figure 2. Conceptual 0.1Hz to 10Hz Noise Testing Scheme Includes Low Noise Pre-Amplifier, Filter and Peak to Peak Noise Detector. Pre-Amplifier's 160nV Noise Floor, Enabling Accurate Measurement, Requires Special Design and Layout Techniques

Numerous details contribute to the circuit's performance. The 1300μF capacitor, a highly specialized type, is selected for leakage in accordance with the procedure given in Appendix B. Further, it, and its associated low noise 1.2k resistor, are fully shielded against pick-up. FETs Q1 and Q2 differentially feed A2, forming a simple low noise op amp. Feedback, provided by the 100k - 10Ω pair, sets closed loop gain at 10,000. Although Q1 and Q2 have extraordinarily low noise characteristics, their offset and drift are uncontrolled. A1 corrects these deficiencies by adjusting Q1's channel current via Q3 to minimize the Q1-Q2 input difference. Q1's skewed drain values ensure that A1 is able to capture the offset. A1 and Q3 supply whatever current is required into Q1's channel to force offset within about 30μV. The FETs' V_{GS} can vary over a 4:1 range. Because of this, they must be selected for 10% V_{GS} matching. This matching allows A1 to capture the offset without introducing significant noise. Q1 and Q2 are thermally mated and lagged in epoxy at a time constant much greater than A1's DC stabilizing loop roll-off, preventing offset instability and hunting. The entire A1-Q1-Q2-A2 assembly and the reference under test are completely enclosed within a shielded can.¹ The reference is powered by a 9V battery to minimize noise and insure freedom from ground loops.

Peak-to-peak detector design considerations include J-FET's used as peak trapping diodes to obtain lower leakage than

afforded by conventional diodes. Diodes at the FET gates clamp reverse voltage, further minimizing leakage.² The peak storage capacitors highly asymmetric charge-discharge profile necessitates the low dielectric absorption polypropylene capacitors specified.³ Oscilloscope connections via galvanically isolated links prevent ground loop induced corruption. The oscilloscope input signal is supplied by an isolated probe; the sweep gate output is interfaced with an isolation pulse transformer. Details appear in Appendix C.

Noise Measurement Circuit Performance

Circuit performance must be characterized prior to measuring LTC6655 noise. The pre-amplifier stage is verified for >10Hz bandwidth by applying a 1μV step at its input (reference disconnected) and monitoring A2's output. Figure 4's 10ms risetime indicates 35Hz response, insuring the entire 0.1Hz to 10Hz noise spectrum is supplied to the succeeding filter stage.

Note 1. The pre-amplifier structure must be carefully prepared. See Appendix A, "Mechanical and Layout Considerations", for detail on pre-amplifier construction.

Note 2. Diode connected J-FET's superior leakage derives from their extremely small area gate-channel junction. In general, J-FET's leak a few picoamperes (25°C) while common signal diodes (e.g. 1N4148) are about 1,000X worse (units of nanoamperes at 25°C).

Note 3. Teflon and polystyrene dielectrics are even better but the Real World intrudes. Teflon is expensive and excessively large at 1μF. Analog types mourn the imminent passing of the polystyrene era as the sole manufacturer of polystyrene film has ceased production.

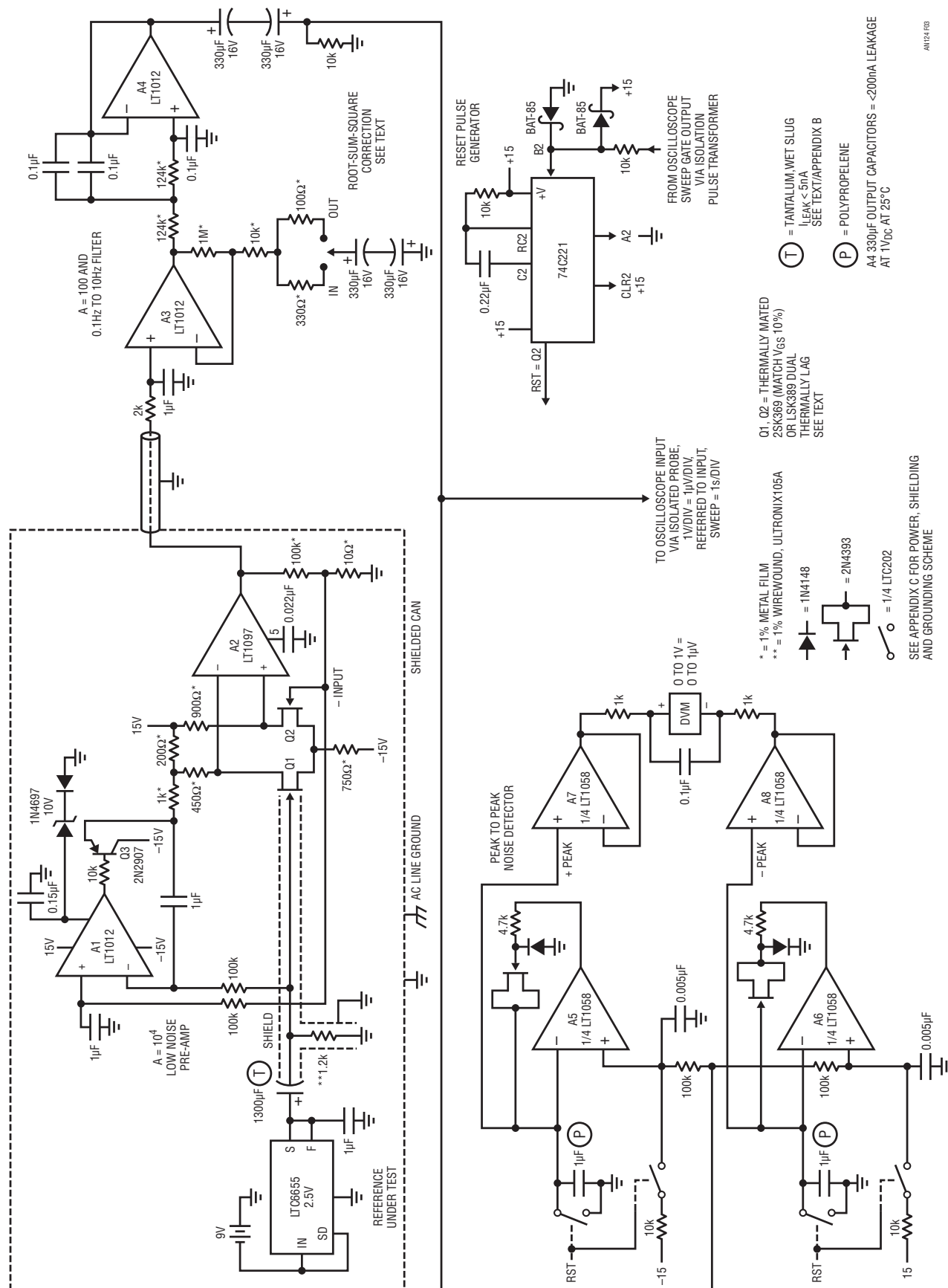


Figure 3. Detailed Noise Test Circuitry. Thermally Lagged Q1-Q2 Low Noise J-FET Pair Is DC Stabilized by A1-Q3; A2 Delivers A = 10,000 Pre-Amplifier Output. A3-A4 form 0.1 Hz to 10 kHz, A = 100, Bandpass Filter; Total Gain Referred to Pre-Amplifier Input Is 10^6 . Peak to Peak Noise Detector, Reset by Monitoring Oscilloscope Sweep Gate, Supplies DVM Output

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Figure 5 describes peak-to-peak noise detector operation. Waveforms include A3's input noise signal (Trace A), A7 (Trace B) positive/A8 (Trace C) negative peak detector outputs and DVM differential input (Trace D). Trace E's oscilloscope supplied reset pulse has been lengthened for photographic clarity.

Circuit noise floor is measured by replacing the LTC6655 with a 3V battery stack. Dielectric absorption effects in the large input capacitor require a 24-hour settling period before measurement. Figure 6, taken at the circuit's oscilloscope output, shows 160nV 0.1Hz to 10Hz noise in a 10 second sample window. Because noise adds in root-sum-square fashion, this represents about a 2% error in

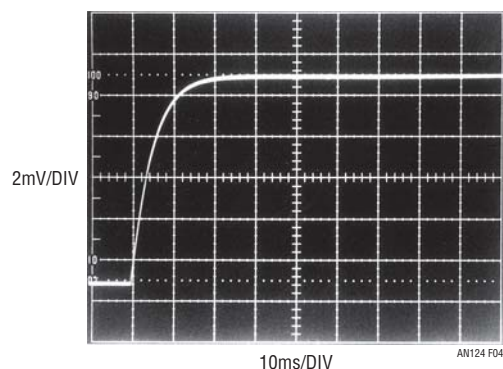


Figure 4. Pre-Amplifier Rise Time Measures 10ms; Indicated 35Hz Bandwidth Ensures Entire 0.1Hz to 10Hz Noise Spectrum Is Supplied to Succeeding Filter Stage

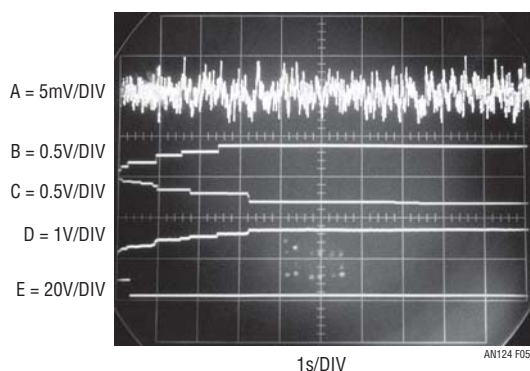


Figure 5. Waveforms for Peak to Peak Noise Detector Include A3 Input Noise Signal (Trace A), A7 (Trace B) Positive/A8 (Trace C) Negative Peak Detector Outputs and DVM Differential Input (Trace D). Trace E's Oscilloscope Supplied Reset Pulse Lengthened for Photographic Clarity

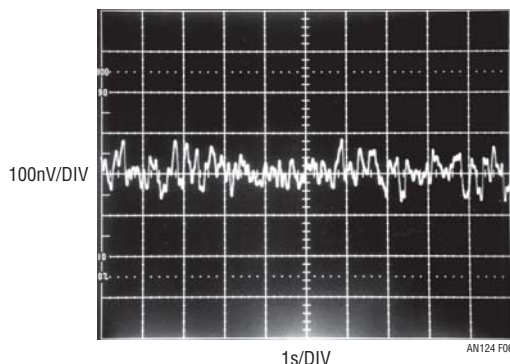


Figure 6. Low Noise Circuit/Layout Techniques Yield 160nV 0.1Hz to 10Hz Noise Floor, Ensuring Accurate Measurement. Photograph Taken at Figure 3's Oscilloscope Output with 3V Battery Replacing LTC6655 Reference. Noise Floor Adds $\approx 2\%$ Error to Expected LTC6655 Noise Figure Due to Root-Sum-Square Noise Addition Characteristic; Correction is Implemented at Figure 3's A3

the LTC 6655's expected 775nV noise figure. This term is accounted for by placing Figure 3's "root-sum-square correction" switch in the appropriate position during reference testing. The resultant 2% gain attenuation first order corrects LTC6655 output noise reading for the circuit's 160nV noise floor contribution. Figure 7, a strip-chart recording of the peak-to-peak noise detector output over 6 minutes, shows less than 160nV test circuit noise.⁴ Resets occur every 10 seconds. A 3V battery biases the input capacitor, replacing the LTC6655 for this test.

Figure 8 is LTC6655 noise after the indicated 24-hour dielectric absorption soak time. Noise is within 775nV peak-to-peak in this 10 second sample window with the root-sum-square correction enabled. The verified, extremely low circuit noise floor makes it highly likely this data is valid. In closing, it is worth mention that the approach taken is applicable to measuring any 0.1Hz to 10Hz noise source, although the root-sum-square error correction coefficient should be re-established for any given noise level.

Note 4. That's right, a *strip-chart recording*. Stubborn, locally based aberrants persist in their use of such archaic devices, forsaking more modern alternatives. Technical advantage could account for this choice, although deeply seated cultural bias may be indicated.

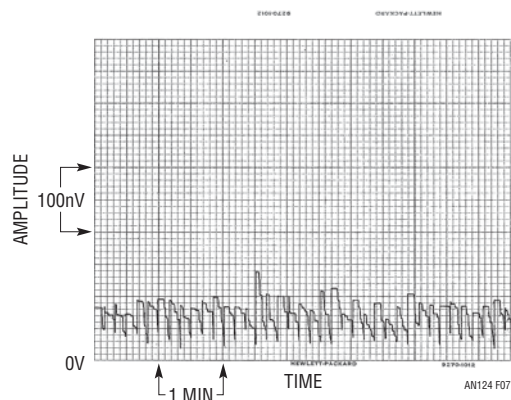


Figure 7. Peak to Peak Noise Detector Output Observed Over 6 Minutes Shows <160nV Test Circuit Noise. Resets Occur Every 10 seconds. 3V Battery Biases Input Capacitor, Replacing LTC6655 for This Test

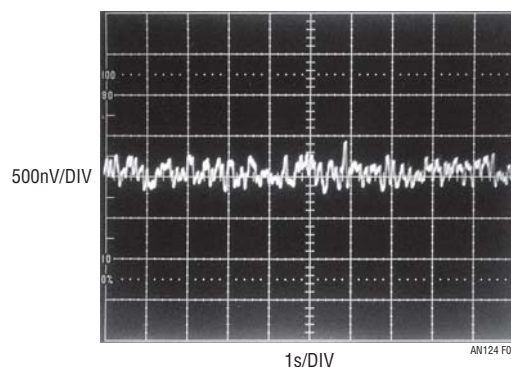


Figure 8. LTC6655 0.1Hz to 10Hz Noise Measures 775nV in 10 Second Sample Time

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6. LT1533 Data Sheet, Linear Technology Corporation.
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APPENDIX A

Mechanical and Layout Considerations

The low noise X10,000 preamplifier, crucial to the noise measurement, must be quite carefully prepared. Figure A1 shows board layout. The board is enclosed within a shielded can, visible in A1A. Additional shielding is provided to the input capacitor and resistor (A1A left); the resistor's wirewound construction has low noise but is particularly susceptible to stray fields. A1A also shows the socketed LTC6655 reference under test (below the large input capacitor shield) and the JFET input amplifier associated components. Q3 (A1A upper right), a heat source, is located away from the JFET printed circuit lands,

preventing convection currents from introducing noise. Additionally, the JFET's are contained within an epoxy filled plastic cup (Figure A1B center), promoting thermal mating and lag.¹ This thermal management of the FETs prevents offset instability and hunting in A1's stabilizing loop from masquerading as low frequency noise. $\pm 15\text{V}$ power enters the enclosure via banana jacks; the reference is supplied by a 9V battery (both visible in A1A). The A = 100 filter and peak-peak detector circuitry occupies a separate board outside the shielded can. No special commentary applies to this section although board leakage to the peak detecting capacitors should be minimized with guard rings or flying lead/Teflon stand-off construction.

Note 1. The plastic cup, supplied by Martinelli and Company, also includes, at no charge, 10 ounces of apple juice.

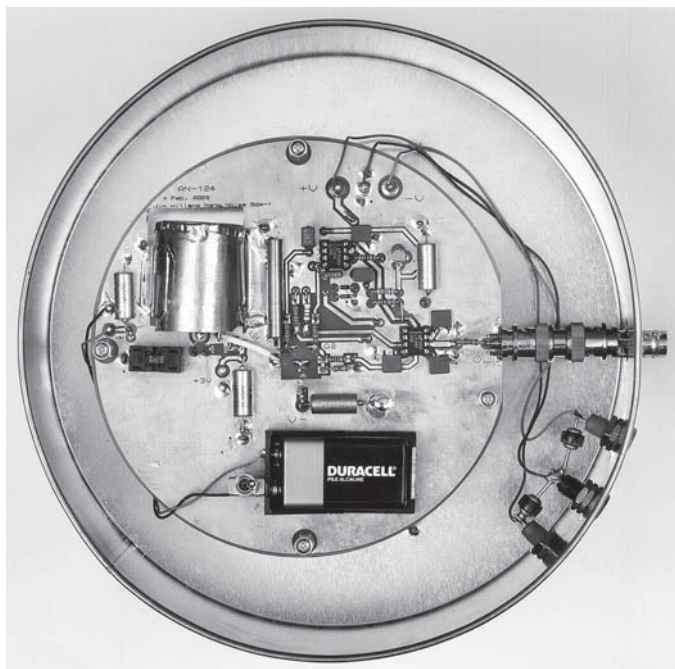


Figure A1A.

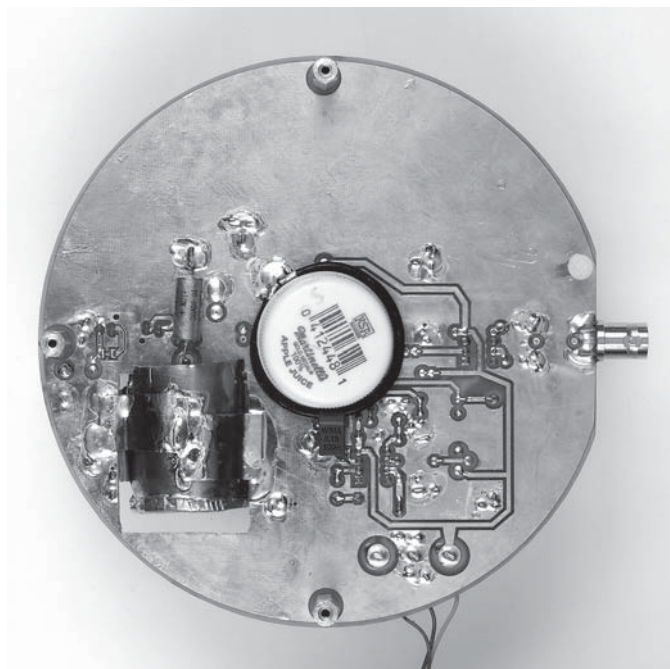


Figure A1B.

Figure A1. Preamplifier Board Top (Figure A1A) and Bottom (A1B) Views. Board Top Includes Shielded Input Capacitor (Upper Left) and Input Resistor (Upper Center Left). Stabilized JFET Input Amplifier Occupies Board Upper Center Right; Output Stage Adjoins BNC Fitting. Reference Under Test Resides in Socket Below Input Capacitor. ± 15 Power Enters Shielded Enclosure Via Banana Jacks (Extreme Right). 9V Battery (Lower) Supplies Reference Under Test. Board Bottom's Epoxy Filled Plastic Cup (A1B Center) Contains JFETs, Provides Thermal Mating and Lag

APPENDIX B

Input Capacitor Selection Procedure

The input capacitor, a highly specialized type, must be selected for leakage. If this is not done, resultant errors can saturate the input pre-amplifier or introduce noise. The highest grade wet slug 200°C rated tantalum capacitors are utilized. The capacitor operates at a small fraction of its rated voltage at room temperature, resulting in much lower leakage than its specification indicates.

The capacitor's dielectric absorption requires a 24-hour charge time to insure meaningful measurement. Capacitor leakage is determined by following the 5-step procedure given in the figure. Yield to required 5-nanoampere leakage exceeds 90%.¹

Note 1. This high yield is most welcome because the specified capacitors are spectacularly priced at almost \$400.00. There may be a more palatable alternative. Selected commercial grade aluminum electrolytics can approach the required DC leakage although their aperiodic noise bursts (mechanism not understood; reader comments invited) are a concern.

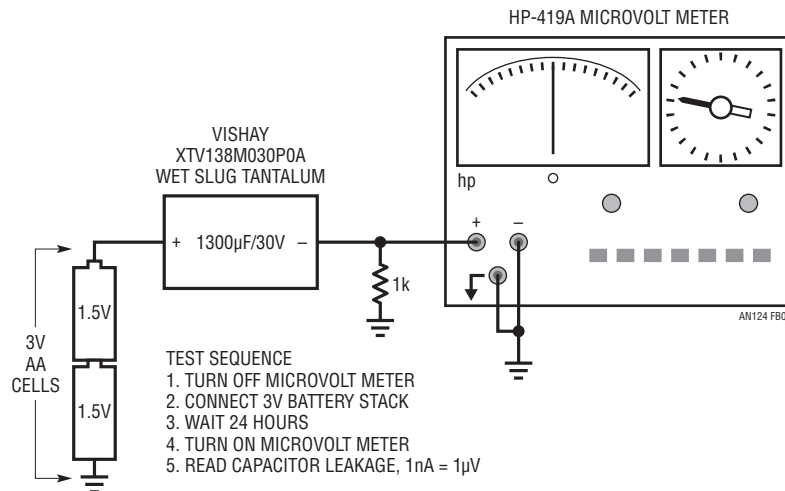


Figure B1. Pre-Amplifier Input Capacitor Selected for <5nA Leakage to Minimize DC Error and Capacitor Introduced Noise. Capacitor Dielectric Absorption Requires 24 Hour Charge Time to Insure Meaningful Measurement. Highest Grade Wet Slug Tantalum Capacitors are Required to Pass This Test

APPENDIX C

Power, Grounding and Shielding Considerations

Figure 3's circuit requires great care in power distribution, grounding and shielding to achieve the reported results. Figure C1 depicts an appropriate scheme. A low shunt capacitance line isolation transformer powers an instrument grade $\pm 15V$ supply, furnishing clean, low noise power. The pre-amplifier's shielded can is tied to the 110V AC ground terminal, directing pick-up to earth ground. Filter/peak-to-peak detector oscilloscope connections are made via an isolated probe and a pulse isolation transformer, precluding error inducing ground loops.¹ The indicated loop, included to verify no current flow between circuit common and earth ground, is monitored with a current probe. Figures C2 and C3, both optional, show battery powered supplies which replace the line isolation transformer and instrumentation

grade power supplies. C2 uses linear regulators to furnish low noise $\pm 15V$. Because the batteries float, positive regulators suffice for both positive and negative rails. In C3, a single battery stack supplies an extremely low noise DC-DC converter to furnish positive and negative rails via low noise discrete linear regulators.² Both of these battery supplied approaches are economical compared to the AC line powered version but require battery maintenance.

The indicated commercial products accompanying Figure C1's blocks represent typical applicable units which have been found to satisfy requirements. Other types may be employed but should be verified for necessary performance.

Note 1. An acceptable alternative to the isolated probe is monitoring Figure 3's A4 output current into a grounded 1k resistor with a DC stabilized current probe (e.g. Tektronix P6042, AM503). The resultant isolated 1V/ μV oscilloscope presentation requires 10Hz lowpass filtering (see Appendix D) due to inherent current probe noise.

Note 2. References 6 and 8 detail the specialized DC-DC converter used.

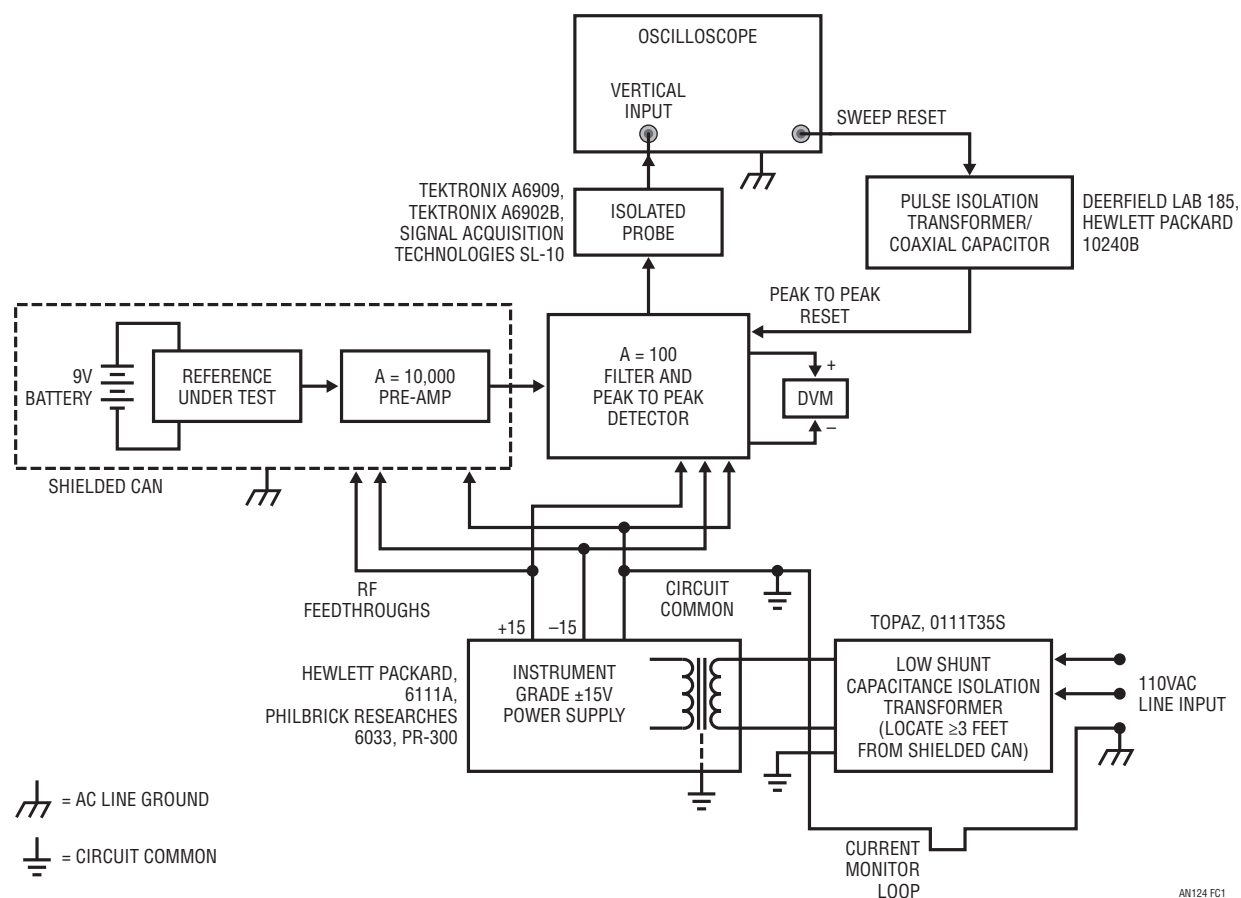


Figure C1. Power/Grounding/Shielding Scheme for Low Noise Measurement Minimizes AC Line Originated Interference and Mixing of Circuit Return and AC Line Ground Current. No Current Should Flow in Current Monitor Loop

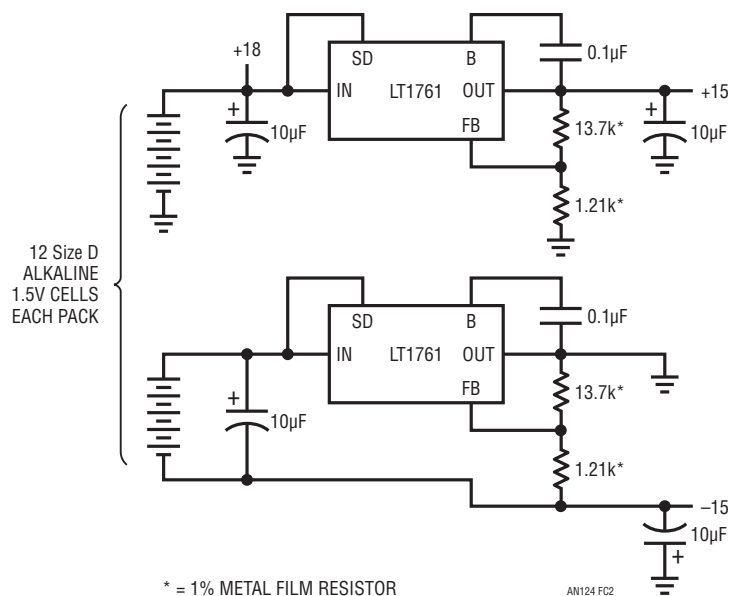


Figure C2. LT1761 Regulators form $\pm 15V$, Low Noise Power Supply. Isolated Battery Packs Permit Positive Regulator to Supply Negative Output and Eliminate Possible AC Line Referred Ground Loops

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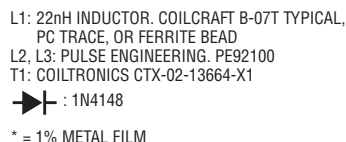


Figure C3. A Low Noise, Bipolar, Floating Output Converter. Grounding LT1533 “DUTY” Pin and Biasing FB Puts Regulator into 50% Duty Cycle Mode. LT1533’s Controlled Transition Times Permit <100µV Broadband Output Noise; Discrete Linear Regulators Maintain Low Noise, Provide Regulation

APPENDIX D

High Sensitivity, Low Noise Amplifiers

Figure D1 lists some useful low level amplifiers for setting up and troubleshooting the texts' circuit. The table lists both oscilloscope plug-in amplifiers and stand-alone types. Two major restrictions apply. The filters in these units

are single-pole types resulting in somewhat pessimistic bandwidth cut-offs. Additionally, the amplifiers listed do not include 10Hz lowpass frequency filters, although they are easily modified to provide this capability. Figure D2 lists four amplifiers with the necessary modification information.¹

Note 1. See References 14-17.

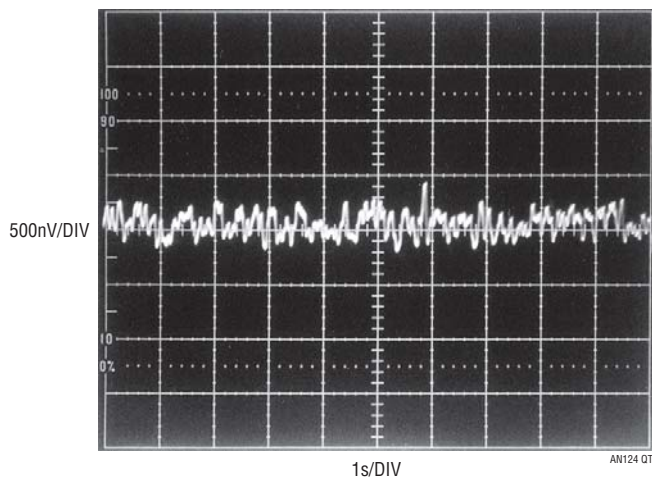
INSTRUMENT TYPE	MANUFACTURER	MODEL NUMBER	-3dB BANDWIDTH	MAXIMUM SENSITIVITY/GAIN	AVAILABILITY	COMMENTS
Differential Amplifier	Tektronix	1A7/1A7A	1MHz	10 μ V/DIV	Secondary Market	Requires 500 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	7A22	1MHz	10 μ V/DIV	Secondary Market	Requires 7000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	5A22	1MHz	10 μ V/DIV	Secondary Market	Requires 5000 Series Mainframe, Settable Bandstops
Differential Amplifier	Tektronix	ADA-400A	1MHz	10 μ V/DIV	Current Production	Stand-Alone with Optional Power Supply, Settable Bandstops
Differential Amplifier	Preamble	1822	10MHz	Gain = 1000	Current Production	Stand-Alone, Settable Bandstops
Differential Amplifier	Stanford Research Systems	SR-560	1MHz	Gain = 50000	Current Production	Stand-Alone, Settable Bandstops, Battery or Line Operation
Differential Amplifier	Tektronix	AM-502	1MHz	Gain = 100000	Secondary Market	Requires TM-500 Series Power Supply, Settable Bandstops

Figure D1. Some Useful High Sensitivity, Low Noise Amplifiers. Trade-Offs Include Bandwidth, Sensitivity and Availability

MANUFACTURER	MODEL NUMBER	MODIFICATION
Tektronix	1A7	Parallel C370A with 1 μ F
Tektronix	1A7A	Parallel C445A with 1 μ F
Tektronix	7A22	Parallel C426H with 3 μ F
Tektronix	AM502	Parallel C449 with 3 μ F

Figure D2. Modification Information for Various Tektronix Low Level Oscilloscope Plug-In's and Amplifiers Permits 10Hz High Frequency Filter Operation in 100Hz Panel Switch Position. All Cases Utilize 100V, Mylar Capacitors

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"...Singeth a quiet tune."

Samuel Coleridge

— The Ancient Mariner
1798