

Analysis and Measurement of Intrinsic Noise in Op Amp Circuits Part VII: Noise Inside The Amplifier

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This TechNote discusses the fundamental physical relationships that determine the intrinsic noise of an operational amplifier (op amp). Board-and-system level designers will gain insight into performance tradeoffs made by integrated circuit designers between noise and other op amp parameters. Also, engineers will learn how to estimate worst case noise based on typical datasheet specifications at room temperature and over temperature.

Five Rules-Of-Thumb For Worst Case Noise Analysis And Design

Most op amp datasheets list only a typical value for noise, with no information regarding temperature drift. Board and system level designers would like to have a method for estimating maximum noise based on the typical value. Furthermore, it would be useful to estimate noise drift with temperature. There are some fundamental noise relationships for transistors that can help to make these estimates. However, in order to make use of these relationships precisely, some knowledge of the internal topology is required (eg biasing configuration, transistor type, etc). Nevertheless, it is possible, if we consider the worst case configuration, to make some general statements that cover the majority of configurations. This section of the TechNote summarizes five basic rules-of-thumb for worst case noise analysis and design. The next section gives detailed mathematics behind these rules-of-thumb.

Rule-Of-Thumb #1: Broadband voltage noise is very insensitive to semiconductor process changes. This is because op amp noise is generally a function of bias current which is typically relatively constant from device to device. Alternatively, for some designs, noise could be dominated by the thermal noise of the input ESD protection resistors. With this in mind, it is unlikely that the broadband noise will change more than 10% from the typical value and is usually less for most low-noise devices (see Fig. 7.1).

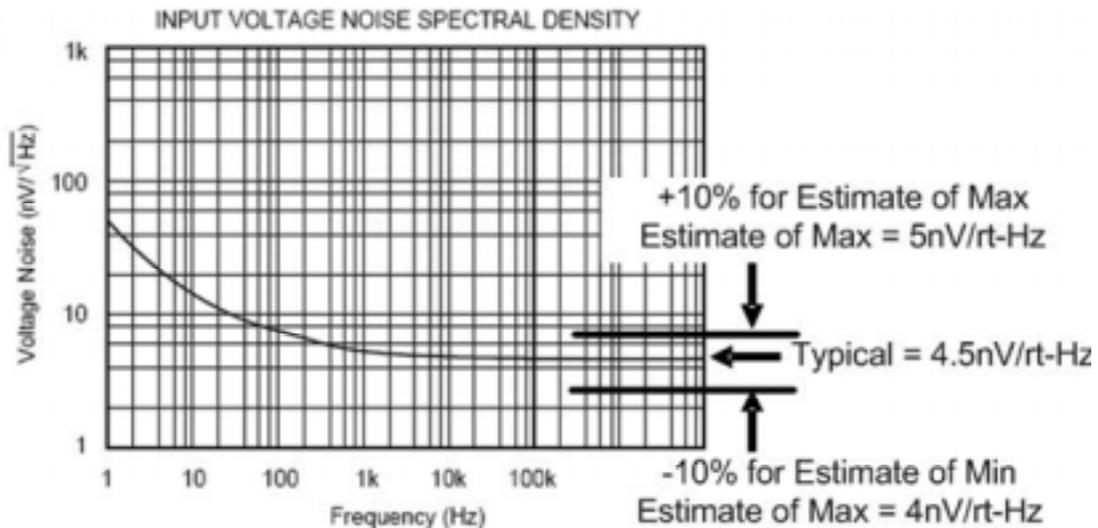


Fig. 7.1: Estimate Max Room Temperature Broadband Noise Based on Typical

Broadband current noise is more sensitive than voltage noise (for bipolar processes). This is because current noise is related to base current, which is set by the transistors current gain (Beta). Normally variation broadband current noise spectral density will be less than 30%.

Rule-Of-Thumb #2: Op amp noise increases with temperature. For many biasing schemes (eg proportionate to absolute temperature, PTAT) the noise will increase proportionate to the square root of absolute temperature and so, the change in noise over the extended industrial temperature range is relatively small (15% for 25 to 125°C). It is possible, however, for some biasing schemes (ie zero-TC) to generate noise that is proportionate to absolute temperature. For this worst case scenario, noise changes 33% over the same temperature range. Fig. 7.2 illustrates this graphically.

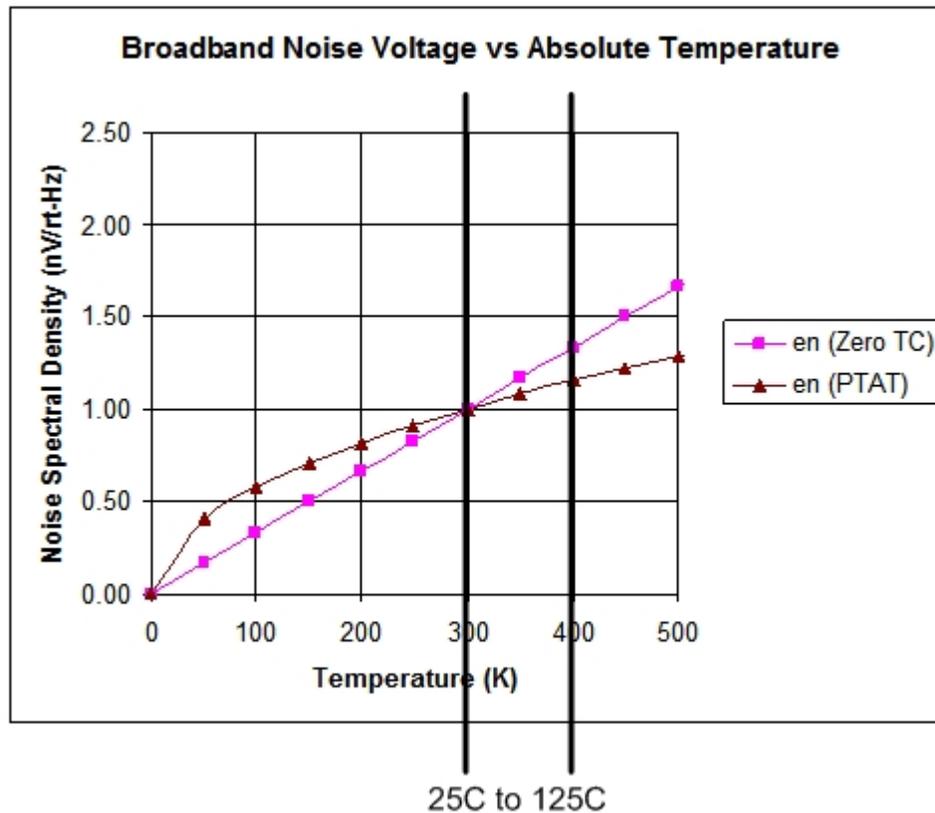


Fig. 7.2: Worst Case And Typical Variations Of Noise Vs Temperature

Rule-Of-Thumb #3: 1/f noise (ie flicker noise) is highly process dependent. This is because 1/f noise is related to defects in the crystalline structure that are created during the fabrication process. So, as long as the semiconductor process is well controlled, the level of 1/f noise should not shift substantially. A fabrication issue or a process change can substantially alter 1/f noise. In cases where the device data sheet gives maximum value for 1/f noise, the process is either monitored or the device is measured at final test. If a data sheet maximum value is not given for 1/f noise, factor of three variations is an estimate for worst case -- assuming that the process control is not optimized for 1/f noise reduction (see Fig. 7.3).

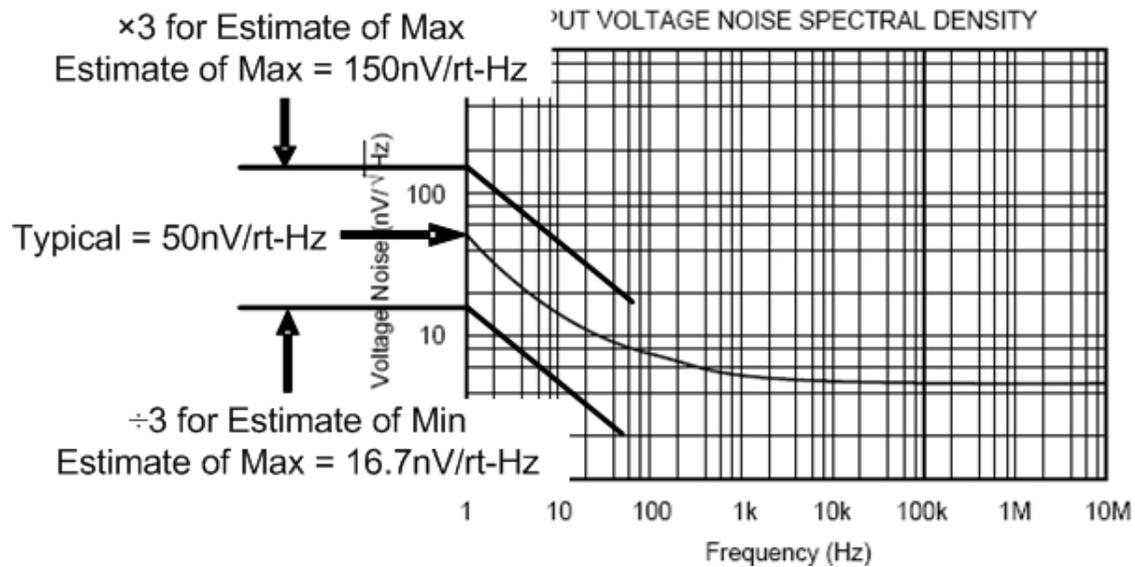


Fig. 7.3: Worst Case Estimate For 1/f Noise

Rule-Of-Thumb #4: Board-and-system level designers need to understand that I_q and broadband noise are inversely related. Strictly speaking, noise is related to the biasing of the op amp's input differential stage. However, since this information isn't normally published, we can assume that I_q is proportionate to the square root of the differential stage bias. This assumption is most accurate with low noise amplifiers, but this relationship can vary for different biasing schemes.

This rule-of-thumb should help board-and-system level designers better understand the tradeoff between I_q and noise. For example, a designer should not expect amplifiers with extremely low quiescent current to also have low noise (see Fig. 7.4).

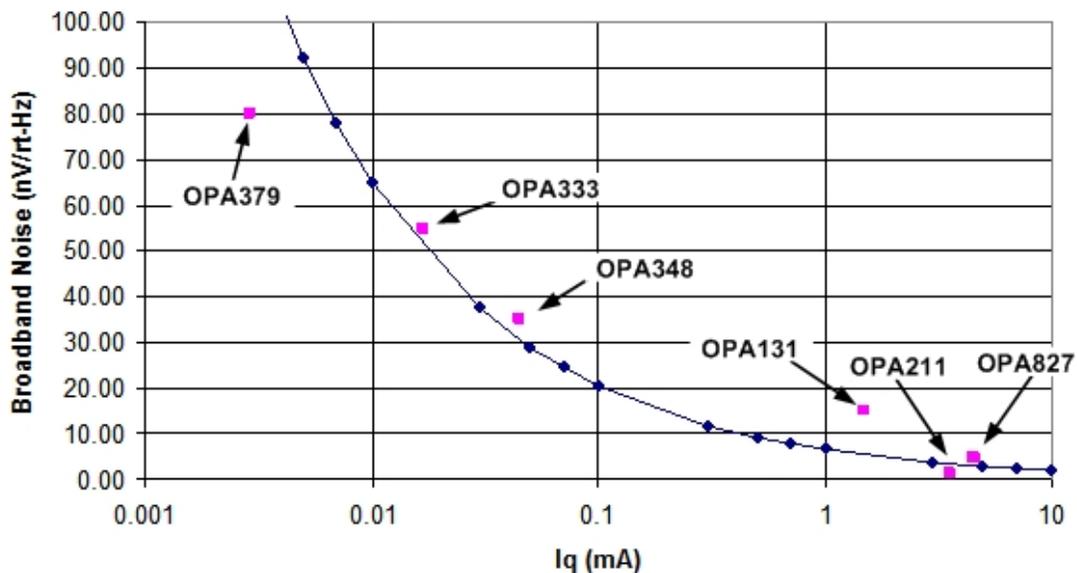


Fig. 7.4: I_q Vs Broadband Noise

Rule-Of-Thumb #5: FET op amps have inherently low current noise. This deals with the difference between bipolar and FET transistors and noise and is because the input gate current of a FET is substantially smaller than the input base current of a bipolar amplifier. Conversely, bipolar amplifiers tend to have lower voltage noise for a given value of bias current (ie collector or drain current on the input stage). See several examples in Fig. 7.5.

op amp	Type	I _q (mA)	i _n (fA/rt-Hz)	e _n (nV/rt-Hz)
OPA277	Bipolar	0.79	200	8
OPA211	Bipolar	3.6	1500	1.1
OPA227	Bipolar	3.7	400	3
OPA348	CMOS	0.045	4	35
OPA364	CMOS	1.1	0.6	17
OPA338	CMOS	0.53	0.6	26

Fig. 7.5: Comparing MOS To Bipolar For Voltage And Current Noise

Detailed Mathematics For Bipolar Noise

Fig. 7.6 illustrates the schematic of the bipolar transistor noise model. The fundamental noise relationships for bipolar transistors are given in Fig. 7.7 with Equations 1, 2, and 3. In this section we manipulate these equations to show the fundamental relationships that are the basis for these rules-of-thumb.

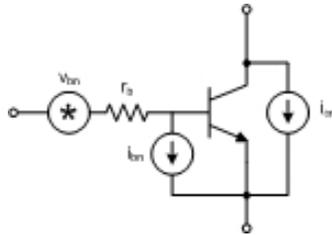


Fig. 7.6: Bipolar Transistor Noise Model

$$v_{bn}^2 = 4 \cdot kT \cdot r_b \cdot \Delta f \quad (1)$$

where

v_{bn} - Thermal noise at base of bipolar transistor from physical resistance

k - Boltzmann's constant (1.381E-23 joule/°K)

T - Temperature in Kelvin

r_b - Physical resistance in base of transistor

Δf - Noise bandwidth

$$i_{cn}^2 = 2 \cdot q \cdot I_C \cdot \Delta f \quad (2)$$

where

i_{cn} - Collector shot noise current

q - Electron charge ($1.6 \cdot 10^{-19}$ coulomb)

I_C - dc collector current

$$i_{bn}^2 = 2 \cdot q \cdot I_B \cdot \Delta f + K_1 \cdot \frac{I_B^a}{f^b} \cdot \Delta f \quad (3)$$

Shot noise Flicker noise Burst noise

where

i_{bn} - Base current noise

I_B - DC base current

K_1 - Semiconductor process dependent constant for flicker noise

a - a constant between 0.5 and 2.0

b - a constant about unity

Fig. 7.7: Fundamental Bipolar Noise Relationships

Analysis Using Equation 1: Bipolar Thermal Noise

Equation 1 represents the physical resistance thermal noise in the base of a bipolar transistor. In an integrated circuit op amp, this resistor often is from an ESD protection circuit in series with the base of the differential input stage (see Fig. 7.8). In some cases this noise dominates.

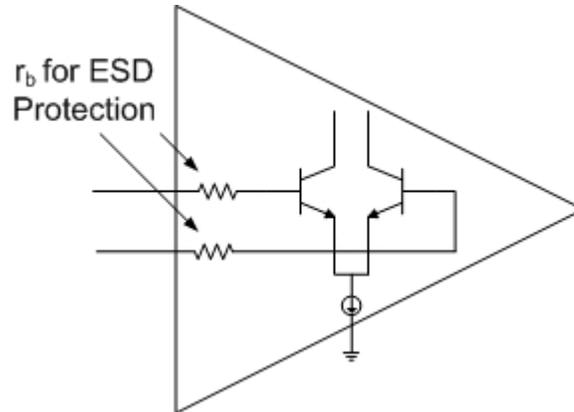


Fig. 7.8: Thermal Noise Component Of Op Amp Noise

For most integrated circuit processes, it is reasonable to assume $\pm 20\%$ tolerance for this resistance. Fig. 7.9 shows that a 20% variation of input resistance corresponds to 10% variation in noise.

$$v_{bn}^2 = 4 \cdot kT \cdot r_b \cdot \Delta f$$

For a 20% variation in r_b v_{bn} will vary

$$\%_variation_vbn = \frac{\sqrt{4 \cdot kT \cdot 1.2 \cdot r_b \cdot \Delta f} - \sqrt{4 \cdot kT \cdot r_b \cdot \Delta f}}{\sqrt{4 \cdot kT \cdot r_b \cdot \Delta f}} \cdot 100$$

$$\%_variation_vbn = \frac{(\sqrt{1.2} - \sqrt{1}) \cdot \sqrt{4 \cdot kT \cdot r_b \cdot \Delta f}}{\sqrt{4 \cdot kT \cdot r_b \cdot \Delta f}} \cdot 100$$

$$\%_variation_vbn = 9.5\%$$

Figure 7.9: Thermal Noise Tolerance

Analysis Using Equation 2: Bipolar Collector Shot Noise

Equation 2 gives the relationship for bipolar transistor collector shot noise. To better understand this relationship, it helps to convert it to a voltage noise v_{cn} (see Fig. 7.10). Further simplifications can be done to the formula, if the biasing scheme for the input stage is known. There are two types of biasing schemes for op amp input stages. One forces the collector current to be proportionate to absolute temperature (PTAT) when the collector current can be represented as a constant multiplied by absolute temperature.

$$i_{cn}^2 = 2 \cdot q \cdot I_c \cdot \Delta f$$

In terms of voltage

$$v_{cn}^2 = \frac{1}{g_m^2} \cdot (2 \cdot q \cdot I_c \cdot \Delta f)$$

Substitute gm for bipolar

$$g_m = \frac{I_c}{V_t} \quad g_m = \frac{I_c}{\frac{k \cdot T}{q}} \quad \frac{1}{g_m} = \frac{k \cdot T}{q \cdot I_c}$$

Collector shot noise in voltage format

$$v_{cn}^2 = \left(\frac{k \cdot T}{q \cdot I_c} \right)^2 \cdot (2 \cdot q \cdot I_c \cdot \Delta f)$$

Fig. 7.10: Convert Current Noise To Voltage Noise

Collector shot noise in voltage format

$$v_{cn}^2 = \left(\frac{k \cdot T}{q \cdot I_c} \right)^2 \cdot (2 \cdot q \cdot I_c \cdot \Delta f)$$

assuming PTAT $I_c = \alpha \cdot T \cdot I_{c0}$

$$v_{cn}^2 = \left[\frac{k \cdot T}{q \cdot (\alpha \cdot T \cdot I_{c0})} \right]^2 \cdot [2 \cdot q \cdot (\alpha \cdot T \cdot I_{c0}) \cdot \Delta f]$$

combine all constants into K_a

$$v_{cn}^2 = K_a \left(\frac{1}{I_c} \right)^2 \cdot [(T \cdot I_c) \cdot \Delta f]$$

$$v_{cn} = \sqrt{\frac{K_a \cdot T \cdot \Delta f}{I_c}}$$

Thus, collector shot noise voltage is directly proportionate to \sqrt{T} and inversely proportionate to $\sqrt{I_c}$ for a PTAT bias.

Fig. 7.11: Collector Noise Voltage For PTAT Bias

Fig. 7.11 shows a simplification of the v_{cn} equation based on a PTAT biasing scheme. The key result is that the noise is directly proportionate to the square root of temperature,

and inversely proportionate to the square root of I_c . This important result illustrates why low-noise amplifiers always have high quiescent current. This is the basis of the fourth rule-of-thumb. The result also shows that the op amp noise increases with temperature. This is the basis of the second rule of thumb. Op amp input stages also are biased in a *Zero-TC* configuration where the collector current bias does not drift with temperature. Fig. 7.12 shows a simplification of the v_{cn} equation based on a Zero-TC bias configuration. The key result is that the noise is directly proportionate to temperature, and inversely proportionate to the square root of I_c . The Zero-TC configuration has a disadvantage over the PTAT method because it is more sensitive to changes in temperature. Note that in the second rule-of-thumb, this is the worst case graph.

assuming Zero-TC I_c is constant over temperature

$$v_{cn}^2 = \left(\frac{k \cdot T}{q \cdot I_c} \right)^2 \cdot (2 \cdot q \cdot I_c \cdot \Delta f)$$

combine all constants into K_b

$$v_{cn}^2 = K_b \left(\frac{T}{I_c} \right)^2 \cdot (I_c \cdot \Delta f)$$

$$v_{cn} = T \sqrt{\frac{K_b \Delta f}{I_c}}$$

Thus, collector shot noise voltage is directly proportionate to T and inversely proportionate to $\sqrt{I_c}$ for a Zero-TC bias.

Fig. 7.12: Collector Noise Voltage For Zero-TC Bias

The result from Figs. 7.11 and 7.12 can be used to determine how much noise changes when I_c is modified. In both cases, noise is inversely proportionate to the square root of I_c . In an integrated circuit op amp design the differential input stage typically dominates the noise. Unfortunately, the data sheet doesn't give information about the biasing of this amplifier. To get a rough estimate assume that the change in I_c is proportionate to the change in I_q . In general, the input stage biasing is better controlled than I_q , so this is a conservative estimate. Fig. 7.13 shows an estimate worst case noise for the OPA227. Note that in this case the variation in I_q has little effect on noise. For most practical designs, this variation will be less than 10%. Note that the first rule-of-thumb is based on that fact that both thermal noise variations and shot noise variations (I_c variations) will be less than 10%.

estimate worst case noise based on I_q variation

$$v_{n_worst_case} = v_{n_typical} \sqrt{\frac{I_{q_worst_case}}{I_{q_typical}}}$$

$$v_{n_worst_case} = 8 \sqrt{\frac{825}{790}} = 8.2 \text{ nV/rt-Hz}$$

Fig. 7.13: Worst Case Noise Based On I_q Variation

Analysis Using Equation 3: Bipolar Base Shot Noise And Flicker Noise

Equation 3 describes bipolar transistor base shot and flicker noise. This noise source is analogous to the current noise in an op amp. This current noise source also converts to a voltage noise (see Fig. 7.14). Analyzing the PTAT and Zero-TC bias configuration is not as straightforward as in the collector current shot noise case. This is because the bias methods are designed to control the collector current and the relationship doesn't follow for the base current. For example, a device with Zero-TC collector current will not have Zero-TC base current because bipolar current gain changes with temperature.

$$i_{bn}^2 = K_1 \cdot \frac{I_B^a}{f} \cdot \Delta f$$

Where K1 is the flicker constant and is process dependent

$$v_{bn}^2 = \frac{1}{\beta_m^2} \left(K_1 \cdot \frac{I_B^a}{f} \cdot \Delta f \right)$$

$$v_{bn}^2 = \left(\frac{k \cdot T}{q \cdot I_c} \right)^2 \left(K_1 \cdot \frac{I_B^a}{f} \cdot \Delta f \right)$$

Combining all constants into Kd

$$v_{bn}^2 = K_d \left(\frac{T}{I_c} \right)^2 \left(\frac{I_B^a}{f} \cdot \Delta f \right)$$

Thus, flicker noise also increases with temperature and decrease with I_c.

Fig. 7.14: Flicker Noise Voltage Relationship

The shot noise component in Equation 3 is responsible for broadband current noise. Note that the noise current is proportional to the square root of I_b. This is why broadband current noise is more sensitive than broadband voltage noise. Variations in I_b are caused by the current gain (beta) of the transistor.

Note that the shot noise component is in the same form as Equation 2. So the analysis is the same, except that the temperature coefficient of the base current is difficult to predict. So, for the sake of simplicity, we will not include temperature information for the i_b shot noise.

The flicker noise component is converted into a voltage noise in Fig. 7.14. Note that flicker noise increases with temperature and decreases with I_c. Flicker noise, however, is very sensitive to process changes, so the variations of flicker constant (K1) may dominate. This is different from the broadband case where the constant was not process dependent. This is the basis for the third rule-of-thumb.

Detailed Mathematics For FET Noise

Fig. 7.15 illustrates the schematic of the MOSFET and JFET transistor noise models. The fundamental noise relationships for FET transistors are given in Fig. 7.16 with Equations 4 and 5. In this section, we manipulate these equations to show that the rules-of-thumb also apply to FET transistors. Fig. 7.17 shows the thermal noise equation being manipulated for PTAT and Zero-TC bias for a FET in strong inversion. Strong inversion refers to the biasing region of the FET. The result of strong inversion is that thermal noise is inversely proportionate to the fourth root of I_d . Thermal noise is directly proportionate to either the square root or fourth root of absolute temperature, depending on the bias type. Thus, the FET amplifier in strong inversion is less sensitive to changes in I_q and temperature than the bipolar amplifier.

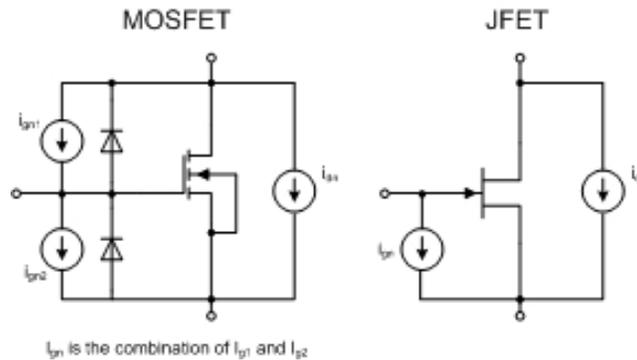


Fig. 7.15: Bipolar Transistor Noise Model

$$i_{gn}^2 = 2 \cdot q \cdot I_G \cdot \Delta f \quad (4)$$

where

i_{gn} - Gate shot noise current

q - Electron charge ($1.6 \cdot 10^{-19}$ coulomb)

I_G - dc gate current (leakage)

Δf - Noise bandwidth

$$i_{dn}^2 = 4 \cdot k \cdot T \cdot \left(\frac{2}{3} \cdot g_m \right) \cdot \Delta f + K_3 \cdot \frac{I_D^a}{f^b} \cdot \Delta f \quad (5)$$

Thermal Noise flicker noise

where

i_{dn} - drain noise from shot noise and flicker noise

k - Boltzmann's constant ($1.381E-23$ joule/ $^{\circ}K$)

T - Temperature in Kelvin

g_m - Transconductance of FET

K_3 - Process dependent constant for flicker noise

Fig. 7.16: Fundamental FET Noise Relationships

$$e_{\text{nbb}} = \sqrt{\frac{2}{3} \frac{4K \cdot T}{g_m}} \quad \text{Broadband noise for FET}$$

$$g_m = \sqrt{2 \cdot K_S \cdot \left(\frac{W}{L}\right) \cdot I_D} \quad \text{for strong inversion}$$

$$e_{\text{nbb}} = \sqrt{\frac{2}{3} \frac{4K \cdot T}{\sqrt{2 \cdot K_S \cdot \left(\frac{W}{L}\right) \cdot I_D}}}$$

Combine all the constants into K_c

$$e_{\text{nbb}} = \sqrt{K_c \frac{T}{\sqrt{I_D}}} \quad \text{Zero-TC equation}$$

Note noise for the Zero-TC bias is proportionate to \sqrt{T}
and inversely proportionate to $\sqrt[4]{I_D}$

For PTAT substitute $I_D = \alpha \cdot I_d$

$$e_{\text{nbb}} = \sqrt{K_c \frac{T}{\sqrt{I_d \cdot \alpha \cdot T}}}$$

Combining all constants into K_d

$$e_{\text{nbb}} = K_d \sqrt[4]{\frac{T}{I_d}}$$

Note noise for the PTAT bias is proportionate to $\sqrt[4]{T}$
and inversely proportionate to $\sqrt[4]{I_D}$

Fig. 7.17: FET In Strong Inversion

Fig. 7.18 shows manipulation of the thermal noise equation for PTAT and Zero-TC bias for a FET in weak inversion. Weak inversion refers to the biasing region of the FET. The result is that thermal noise is inversely proportionate to the square root of I_D . Thermal noise is directly proportionate to temperature, or the square root of temperature, depending on the bias type. Thus, the FET amplifier in weak inversion has relationships similar to a bipolar bias amplifier for current and temperature.

$$i_{nbb}^2 = 4k \cdot T \cdot \left(\frac{2}{3} \cdot g_m \right) \quad \text{Broadband noise}$$

$$g_m = \frac{q \cdot A \cdot I_D}{k \cdot T} \quad \text{For weak inversion}$$

$$e_{nbb}^2 = \frac{1}{2} \cdot \left[4k \cdot T \cdot \left(\frac{2}{3} \cdot g_m \right) \right]$$

$$e_{nbb}^2 = \frac{8k \cdot T}{3 \cdot \frac{q \cdot A \cdot I_D}{k \cdot T}}$$

$$e_{nbb}^2 = \frac{8k^2 \cdot T^2}{3q \cdot A \cdot I_D}$$

$$e_{nbb} = K_c \frac{T}{\sqrt{I_D}} \quad \text{for Zero-TC}$$

$$\text{for Ptat } I_D = \alpha \cdot I_d$$

$$e_{nbb}^2 = K_c \frac{T^2}{\alpha \cdot T \cdot I_d}$$

$$e_{nbb} = K_d \sqrt{\frac{T}{I_d}} \quad \text{for PTAT}$$

Fig. 7.18: FET In Weak Inversion

Fig. 7.19 shows the flicker noise equation being manipulated for PTAT and Zero-TC bias for a FET in strong inversion. Note that "a" is a constant between 0.5 and 2. Thus, it is possible that flicker noise is proportionate to I_D , or inversely proportionate to some power of I_D depending on the value of "a." For a Zero-TC biasing scheme, the value of flicker noise is not dependent on temperature. For a PTAT biasing scheme, the flicker noise will be proportionate to the square root of temperature.

$$e_{dn}^2 = K_3 \cdot \frac{I_D^a}{g_m^2 f^b} \cdot \Delta f \quad \text{General FET flicker equation in voltage form}$$

$$g_m = \sqrt{2 \cdot K_S \cdot \left(\frac{W}{L}\right) \cdot I_D} \quad \text{for strong inversion}$$

$$e_{dn} = K_3 \cdot \sqrt{\frac{I_D^{a-1}}{f^b} \cdot \Delta f} \quad \text{for strong inversion}$$

Fig. 7.19: FET Flicker Noise In Strong Inversion

Fig. 7.20 shows the flicker noise equation being manipulated for PTAT and Zero-TC bias for a FET in weak inversion. Note that "a" is, again, a constant between 0.5 and 2. So, for all cases, flicker noise is inversely proportionate to some power of I_D . For a Zero-TC bias, the flicker noise will be proportionate to absolute temperature. For a PTAT bias the temperature relationship is dependent on the value of "a."

$$e_{dn}^2 = K_3 \cdot \frac{I_D^a}{g_m^2 f^b} \cdot \Delta f \quad \text{General FET flicker equation in voltage form}$$

$$g_m = \frac{q \cdot A \cdot I_D}{k \cdot T} \quad \text{For weak inversion}$$

$$e_{dn} = K_3 \cdot \sqrt{\frac{(I_D^{a-2}) \cdot T^2}{f^b} \cdot \Delta f} \quad \text{For weak inversion}$$

Fig. 7.20: FET Flicker Noise In Weak Inversion

Summary and Preview

In this TechNote, we discussed some rules-of-thumb that help to estimate the worst case noise and the noise over temperature. The rules-of-thumb also help board and system level designers gain insight into the tradeoffs that integrated circuit designers make in low-noise designs. The detailed mathematics behind the rules-of-thumb are also given. Part VIII will focus on a deeper look at 1/f noise and popcorn noise.

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References

Paul R Gray, and Robert G Meyer, *Analysis and Design of Analog Integrated Circuits*, 3rd Edition, Hamilton Printing Company

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