D2676, OCTOBER 1982—REVISED NOVEMBER 1986

- Each Device Drives 10 Lines
- 60-V Output Voltage Rating
- 40-mA Output Source Current
- High-Speed Serially-Shifted Data Input
- CMOS-Compatible Inputs
- Latches on All Driver Outputs
- Designed to be Interchangeable with Sprague UCN4810A

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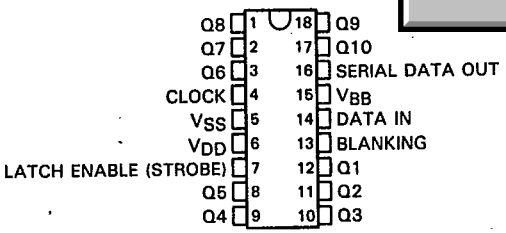
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

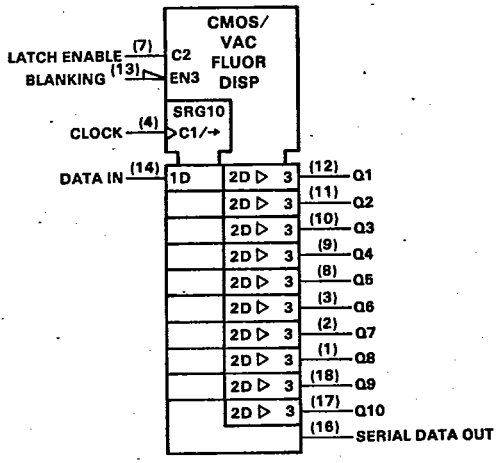
The UCN4810A is a monolithic BIDFET† integrated circuit designed to drive a dot matrix or segmented vacuum fluorescent display (VFD). This device features a serial data output to cascade additional devices for large display arrays.

A 10-bit data word is serially loaded into the shift register on the positive-going transitions of the clock. Parallel data is transferred to the output buffers through a 10-bit D-type latch while the latch enable input is high and will be latched when the latch enable is low. When the blanking input is high, all outputs are low.

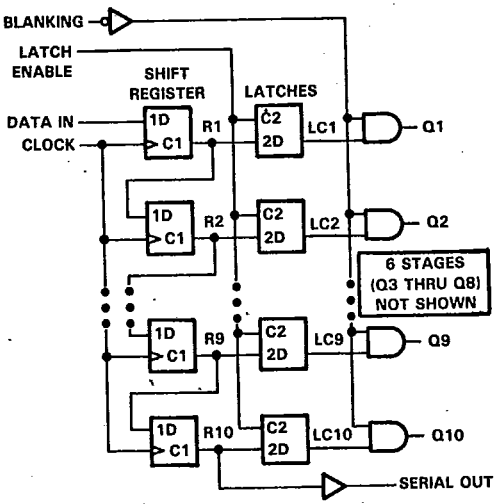
Outputs are totem-pole structures formed by n-p-n emitter-follower and double-diffused MOS (DMOS) transistors with output voltage ratings of 60 volts, and 40 milliamperes source-current capability. All inputs are compatible with CMOS and TTL levels, but each requires the addition of a pull-up resistor to V_{DD} when driven by TTL logic.

The UCN4810A is characterized for operation from 0°C to 70°C.

logic symbol‡



logic diagram (positive logic)



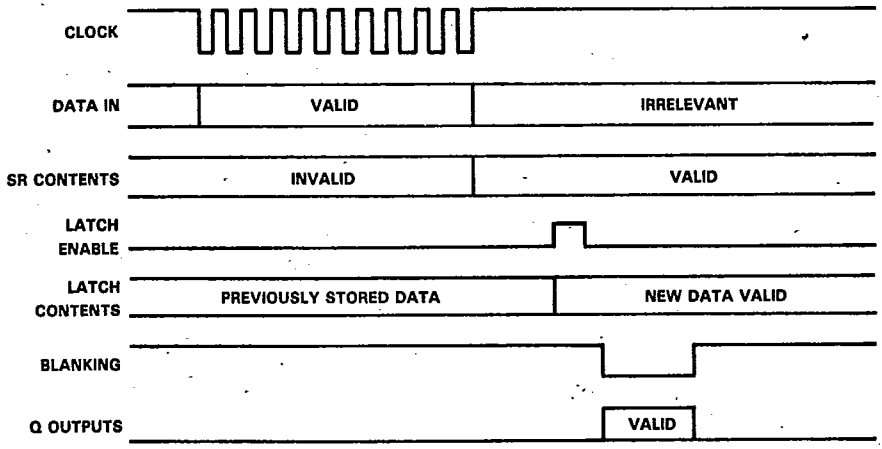
†BIDFET—Bipolar Double-Diffused, N-Channel and P-Channel MOS transistors on same chip—patented process.
‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

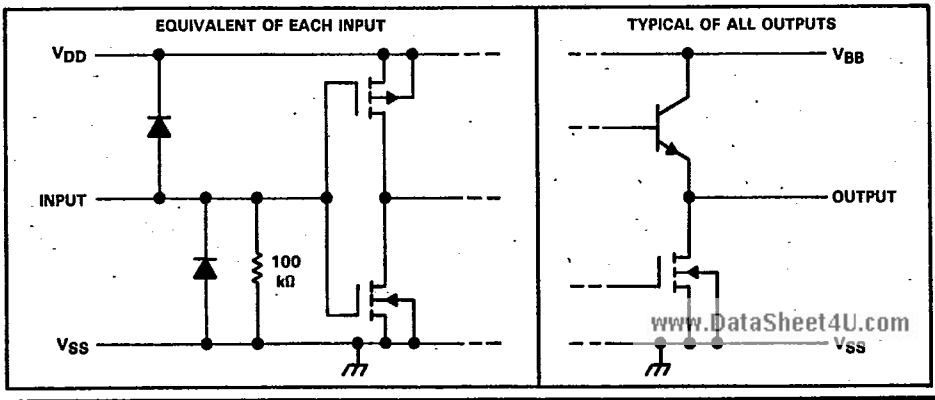
FUNCTION	CONTROL INPUTS			SHIFT REGISTERS R1 THRU R10	LATCHES LC1 THRU LC10†	OUTPUTS	
	CLOCK	LATCH ENABLE	BLANK-ING			SERIAL	Q1 THRU Q10
LOAD	↑	X	X	Load and shift*	Determined by Latch Enable†	R10*	Determined by Blanking
	No ↑	X	X	No change	Determined by Latch Enable†	R10	Determined by Blanking
LATCH	X	L	X	As determined above	Stored data	R10	Determined by Blanking
	X	H	X	As determined above	New data	R10	Determined by Blanking
BLANK	X	X	H	As determined above	Determined by Latch Enable†	R10	All L
	X	X	L	As determined above	Determined by Latch Enable†	R10	LC1 thru LC12 respectively

H = high level, L = low level, X = irrelevant, ↑ = low-to-high-level transition.
†New data enter the latches while Latch Enable is high. These data are stored while Latch Enable is low.
*R10 takes on the state of R9, R9 takes on the state of R8 . . . R2 takes on the state of R1, and R1 takes on the state of the data input.

typical operating sequence



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{DD} (see Note 1) . . . . . 18 V
Driver supply voltage, V_{BB} . . . . . 60 V
Output voltage . . . . . 60 V
Input voltage . . . . . −0.3 V to V_{DD} +0.3 V
Continuous output current . . . . . −40 mA
Continuous total dissipation at 25°C free-air temperature (see Note 2) . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to V_{SS}.
2. For operation above 25°C free-air temperature, derate linearly to 736 mW at 70°C at the rate of 9.2 mW/°C.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.75		15.75	V
Supply voltage, V_{BB}		5		60	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}	for V_{DD} = 5 V	3.5		5.3	V
	for V_{DD} = 15 V	13.5		15.3	
Low-level input voltage, V_{IL}		−0.3†		0.8	V
Continuous high-level output current, I_{OH}				−25	mA
Operating free-air temperature, T_A		0		70	°C

† The algebraic convention, in which the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics, V_{DD} = 4.75 V to 15.75 V, V_{BB} = 60 V, V_{SS} = 0, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −25 mA		57.5		V
V_{OL}	Low-level output voltage	I_{OL} = 1 μA,	Blanking input at V_{DD}		1	V
I_{OL}	Low-level output current (pull-down current)	V_O = 60 V,	Blanking input at V_{DD}	0.4	0.85	mA
$I_{O(off)}$	Off-state output current	V_O = 60 V, All other terminals open,	V_{SS} = 0 V, T_A = 70°C		15	μA
I_{IH}	High-level input current	V_{DD} = 5 V,	V_I = 5 V		0.1	mA
		V_{DD} = 15 V,	V_I = 15 V		0.3	
r_i	Input resistance	V_{DD} = 5 V		50		kΩ
r_o	Output resistance	V_{DD} = 5 V			20	kΩ
		V_{DD} = 15 V			6	
I_{BB}	Supply current from V_{BB}	All outputs high			13	mA
		All outputs low			1.3	
I_{DD}	Supply current from V_{DD}	All inputs at 0 V, One output high	V_{DD} = 5 V		1	mA
			V_{DD} = 15 V		3	
		All inputs at 0 V, All outputs low	V_{DD} = 5 V		0.1	
			V_{DD} = 15 V		0.2	

timing requirements for V_{DD} = 5 V and V_{DD} = 15 V, T_A = 0°C to 70°C

PARAMETER	V_{DD} = 5 V		V_{DD} = 15 V		UNIT
	MIN	MAX	MIN	MAX	
Pulse duration, clock high, $t_{w(CKH)}$	1000		250		ns
Pulse duration, latch enable high, $t_{w(LEH)}$	500		300		ns
Setup time, data before clock ↑, $t_{su(D)}$	250		150		ns
Hold time, data after clock ↑, $t_{h(D)}$	250		150		ns
Delay time, clock ↑ to latch enable high, $t_{CKH-LEH}$	1000		400		ns

switching characteristics, V_{DD} = 5 V or 15 V, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay time, latch enable to output		1		μs

PARAMETER MEASUREMENT INFORMATION

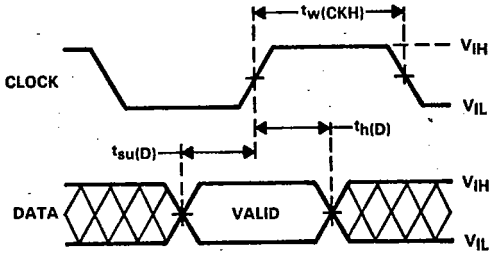


FIGURE 1. INPUT TIMING

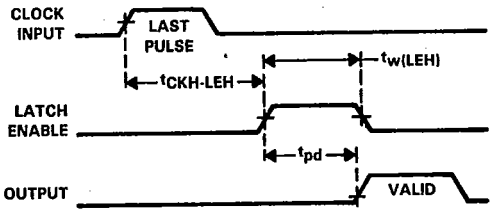


FIGURE 2. OUTPUT SWITCHING TIMES

THERMAL INFORMATION